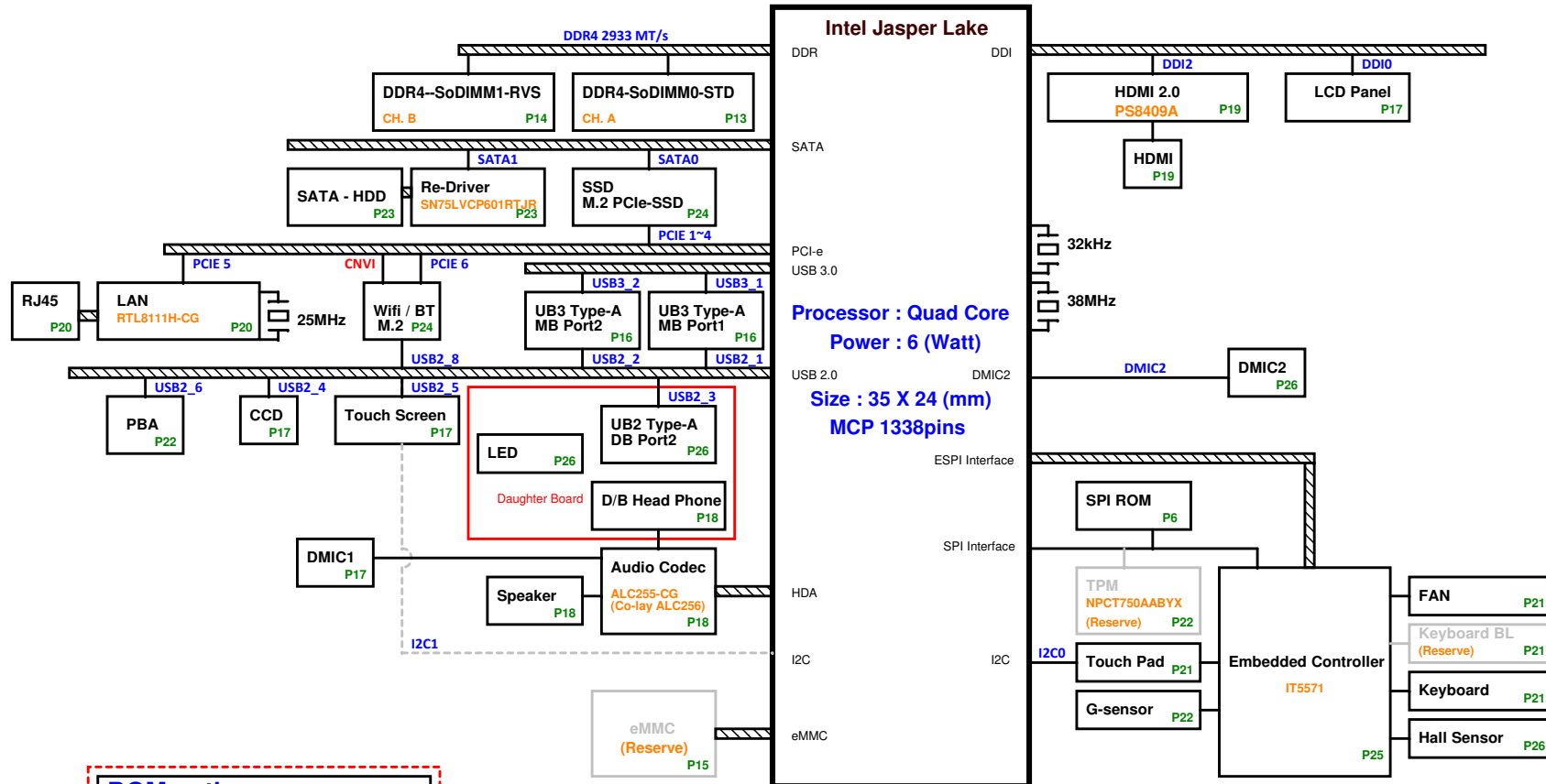


Z8Y Intel JSL Platform Block Diagram

01

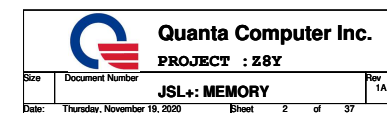


BOM option

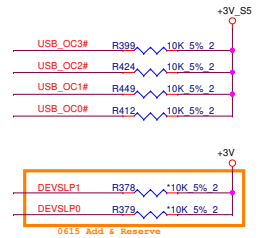
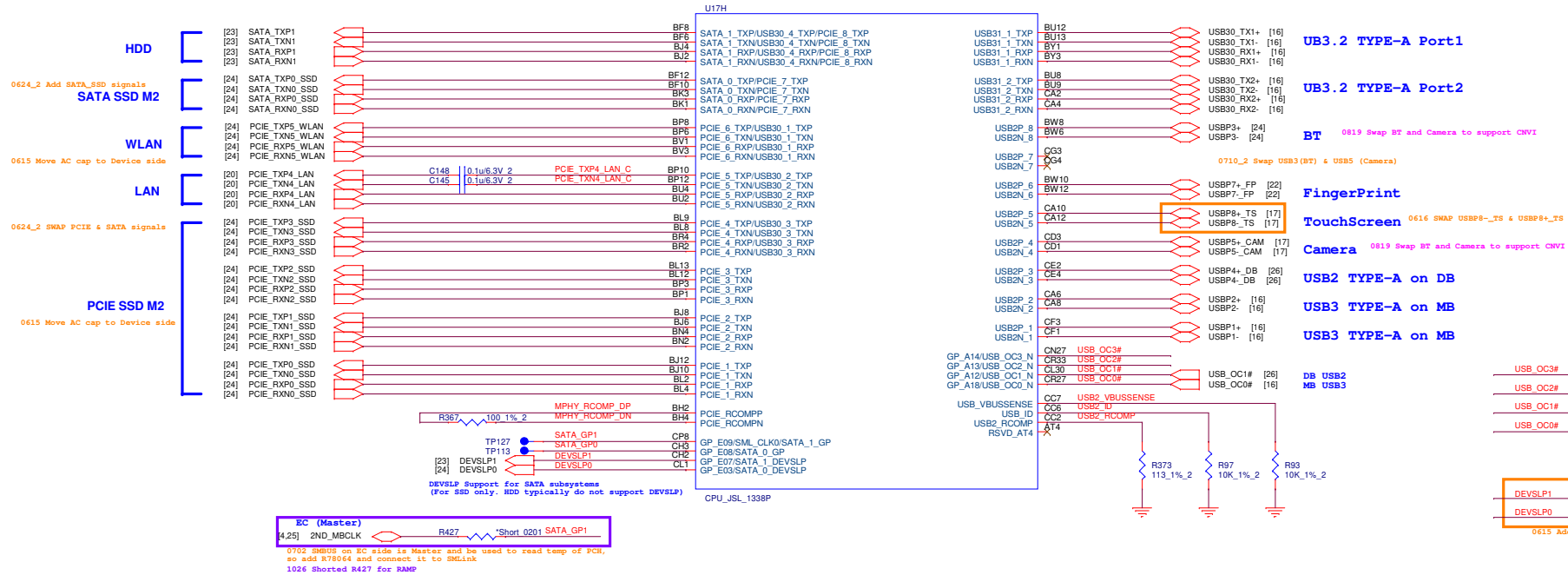
HDD@ : Hard Disk Drive
SSD@ : Solid-state disk
P_SSD@ : PCIe Solid-state disk
S_SSD@ : SATA Solid-state disk
TSi@ : Touch screen I2C
TSU@ : Touch screen USB
PBA@ : Finger Print on touch pad
MMC@ : eMMC function
MMC_N@ : No eMMC function
TPM@ : Trusted Platform Module
TPM_N@ : No Trusted Platform Module
GS@ : G-Sensor function
GS_N@ : No G-Sensor function
KBL@ : Keyboard back light
DBG@ : for Debug Function
DMIC@ : Dual MIC
255@ : Codec ALC255
255M@ : Codec ALC255M (Only for Board ID7)
256@ : Codec ALC256
FOR15@ : Panel 15" project
FOR14@ : Panel 14" project
TS@ : TouchScreen
TMS@ : TouchScreen & Modern Standby
TNMS@ : Touch Screen & Non-Modern Standby
MS@ : Modern Standby
NMS@ : Non Modern Standby

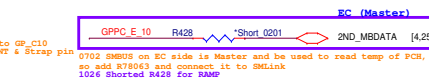
Battery Charger BQ24780SRUYR P27	+VNN_EXT SVV659LQWC P30	+2.5V_SUS JWS252SOTB#TRPB P31	+1.8V AOSS32334C P34	+VCCST DMG3414U-7 P12
+3VPCU/+5VPCU RT6256BGQUF P28	+1.05V_EXT SVV659LQWC P30	+1.2V AOSS32334C P31	+1.5V JWS252SOTB#TRBP P34	
+3V_S5/+5V_S5 AOZ1331ADI P28	+1.2VSUS RT8231BGQW P31	+VCCIN RT3612EBGQW P32	+VCCPLL_OC DMG3414U-7 P12	
+3V/+5V AOZ1331ADI P28	+VDDQ_VTT RT8231BGQW P31	+VCCIN_AUX RT6543AGQW P33	+VCC1P8A DMG3414U-7 P12	
+VCCIO G5335QT2U P29	+VDDQ RT8231BGQW P31	+1.8V_S5 JWS213DFND_TRPB P34	Thermal protection TMP708AIDBVR P34	

Power solution



[2,5,7,9,12,20,21,24,25,28,29,30,31,33,34] +3V_SS
[4,5,7,8,13,14,15,17,18,19,20,21,22,23,24,25,26,28,29,31,32,34] +3V





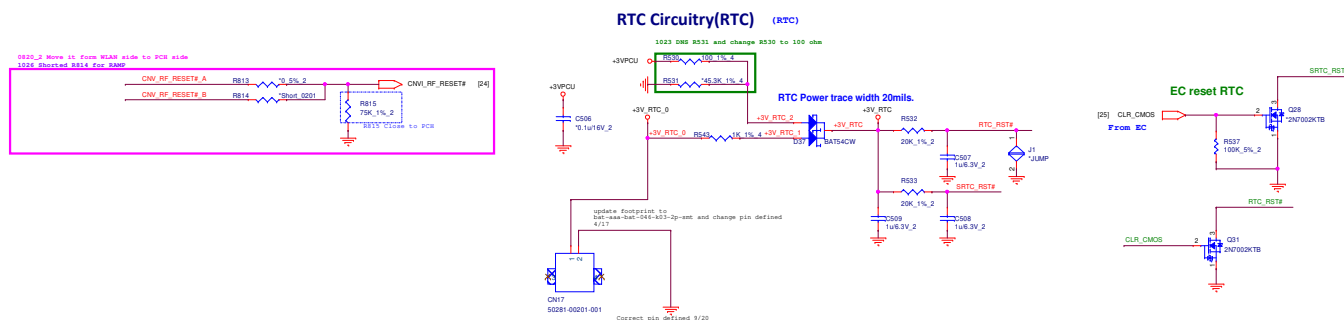
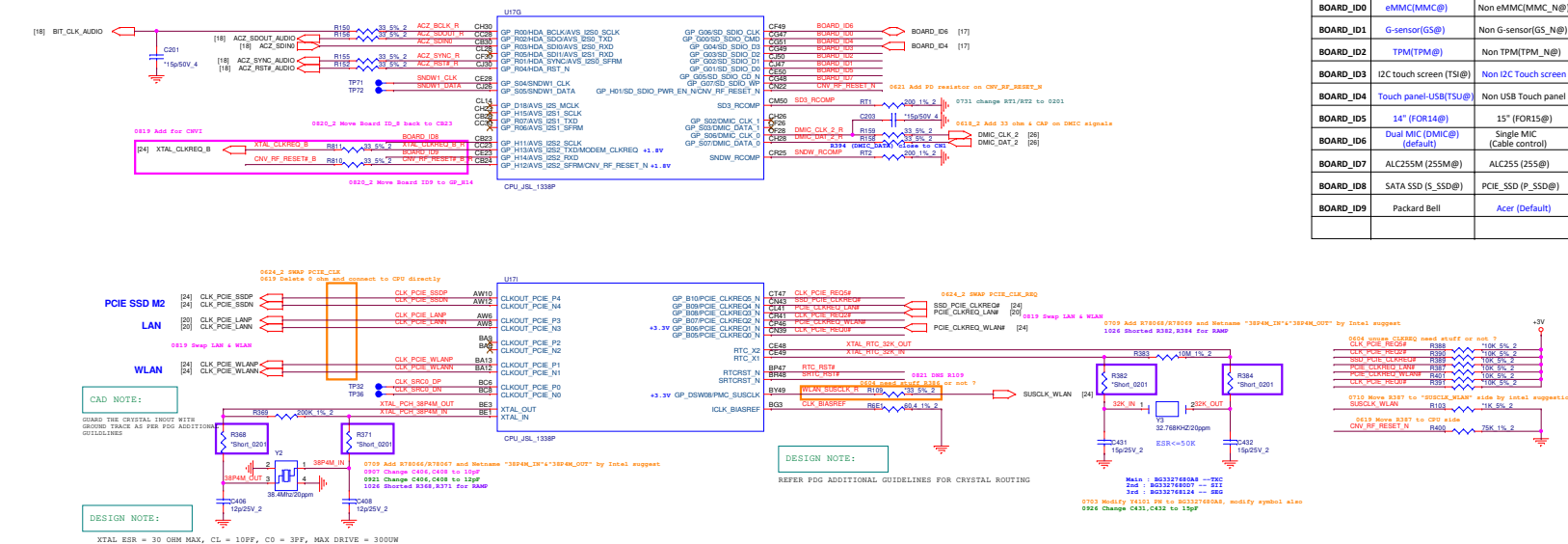


	High	Low
BOARD_ID0	eMMC(MMC@)	Non eMMC(MMC_
BOARD_ID1	G-sensor(G5@)	Non G-sensor(G5_
BOARD_ID2	TPM(TPM@)	Non TPM(TPM_
BOARD_ID3	I2C touch screen (TS@)	Non I2C Touch scr
BOARD_ID4	Touch panel-USB(TSU@)	Non USB Touch pa
BOARD_ID5	14" (FOR14@)	15" (FOR15@)
BOARD_ID6	Dual MIC (DMIC@ (default))	Single MIC (Cable control)
BOARD_ID7	ALC255M (255M@)	ALC255 (255@)
BOARD_ID8	SATA SSD (S_SSD@)	PCIe SSD (P_SSD@)
BOARD_ID9	Packard Bell	Acer (Default)

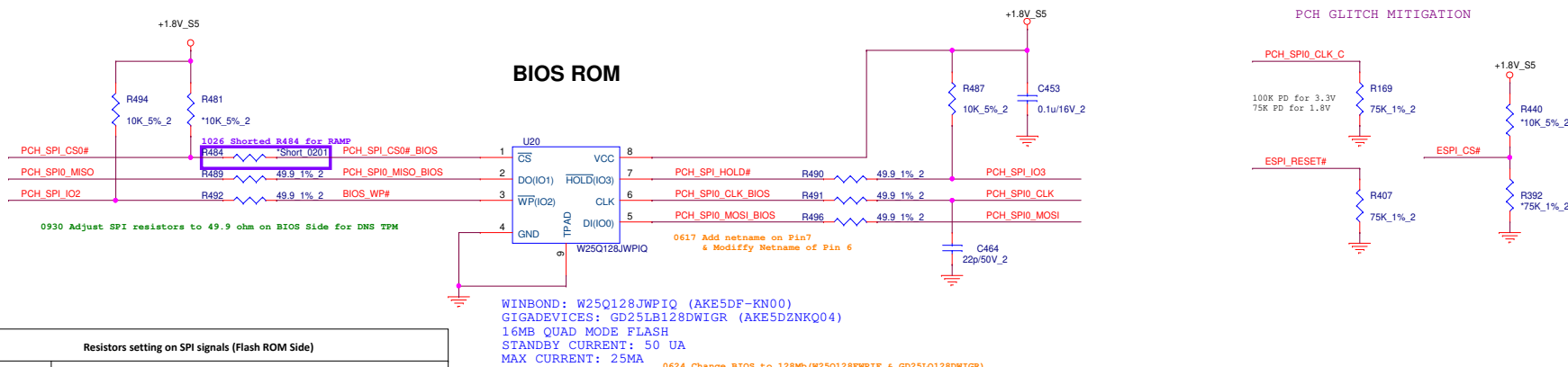
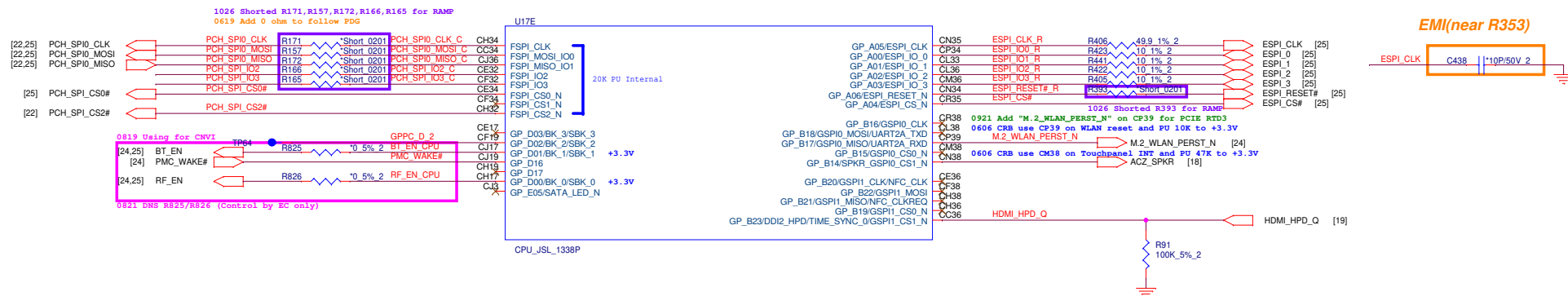
```

1026 Set default to Dual Mi
0813 Add 255g/256g on Board
0703 Delete Board ID7
(DALI & R3 PICASSO) setting
1014 Add Packard Bell / Ace
setting on Board ID 9

```



(CPU)



Resistors setting on SPI signals (Flash ROM Side)

With TPM	15 ohm (CS01501FE09) on CLK,MISO,MOSI : R491,R496,R489 33 ohm (CS03301JE09) on IO2,IO3: R490,R492
Without TPM	49.9 ohm (CS04991FE00) on CLK,MOSI,MISO,IO2,IO3: R491,R496,R489,R490,R492

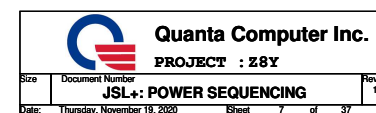
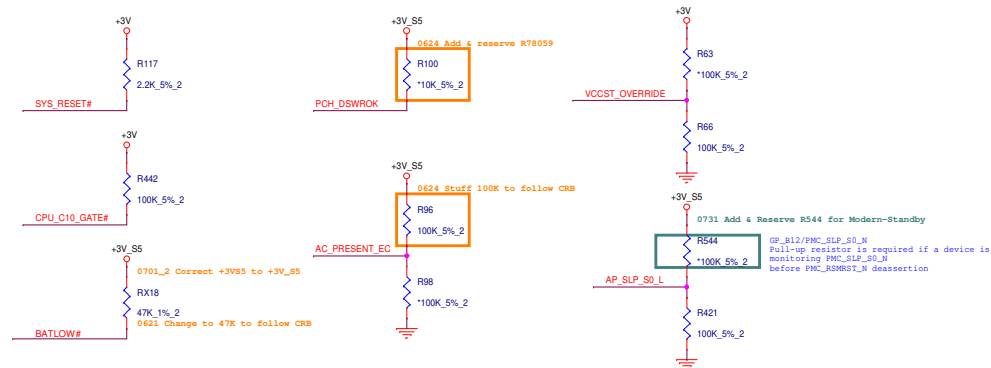


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PROJECT : Z8Y

JSL+: ESPI, SPI

[2,3,5,9,12,20,21,24,25,28,29,30,31,33,34] +3V_S5
[3,4,5,8,13,14,15,17,18,19,20,21,22,23,24,25,26,28,29,31,32,34] +3V
[9,11,12,27,32] +VCCST

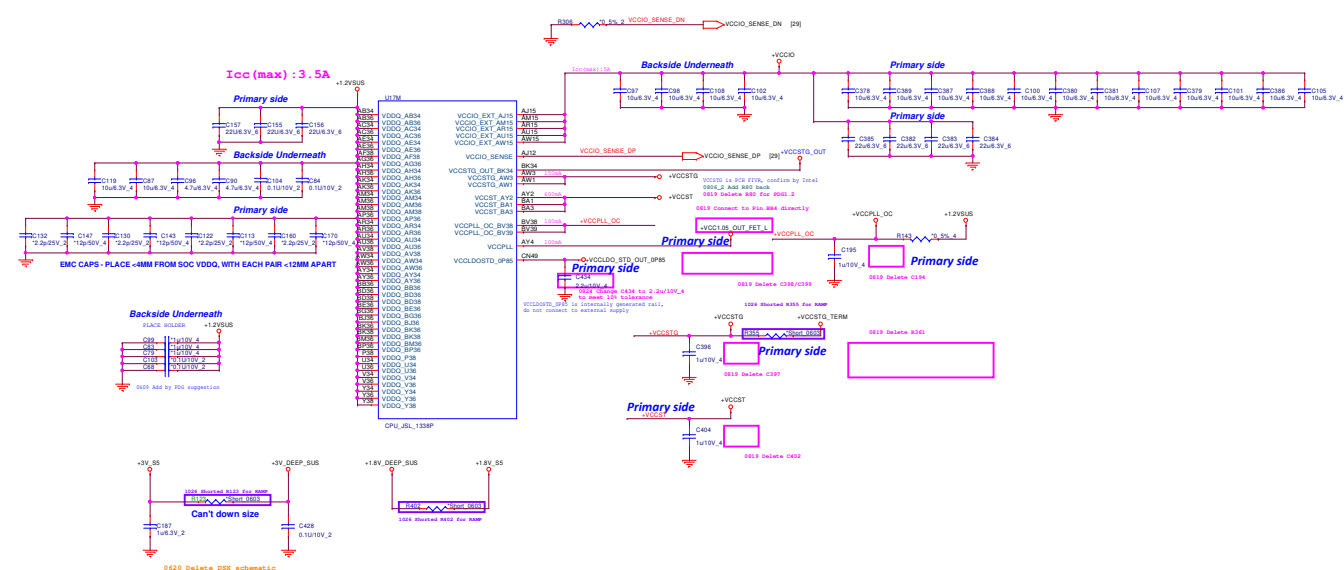
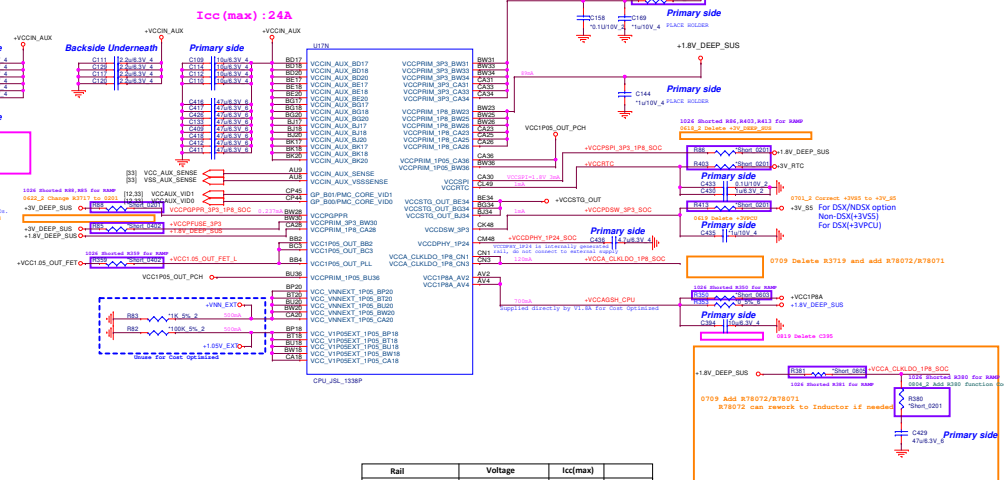
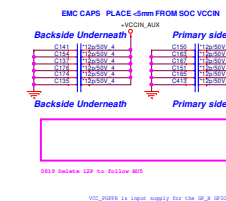
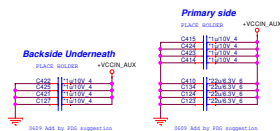


(CPU)



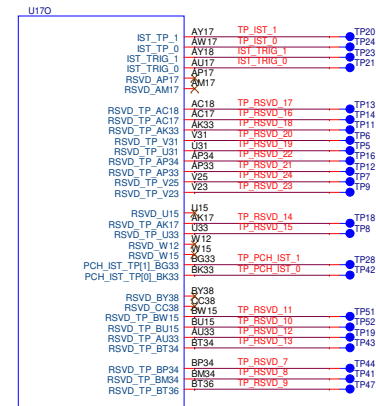
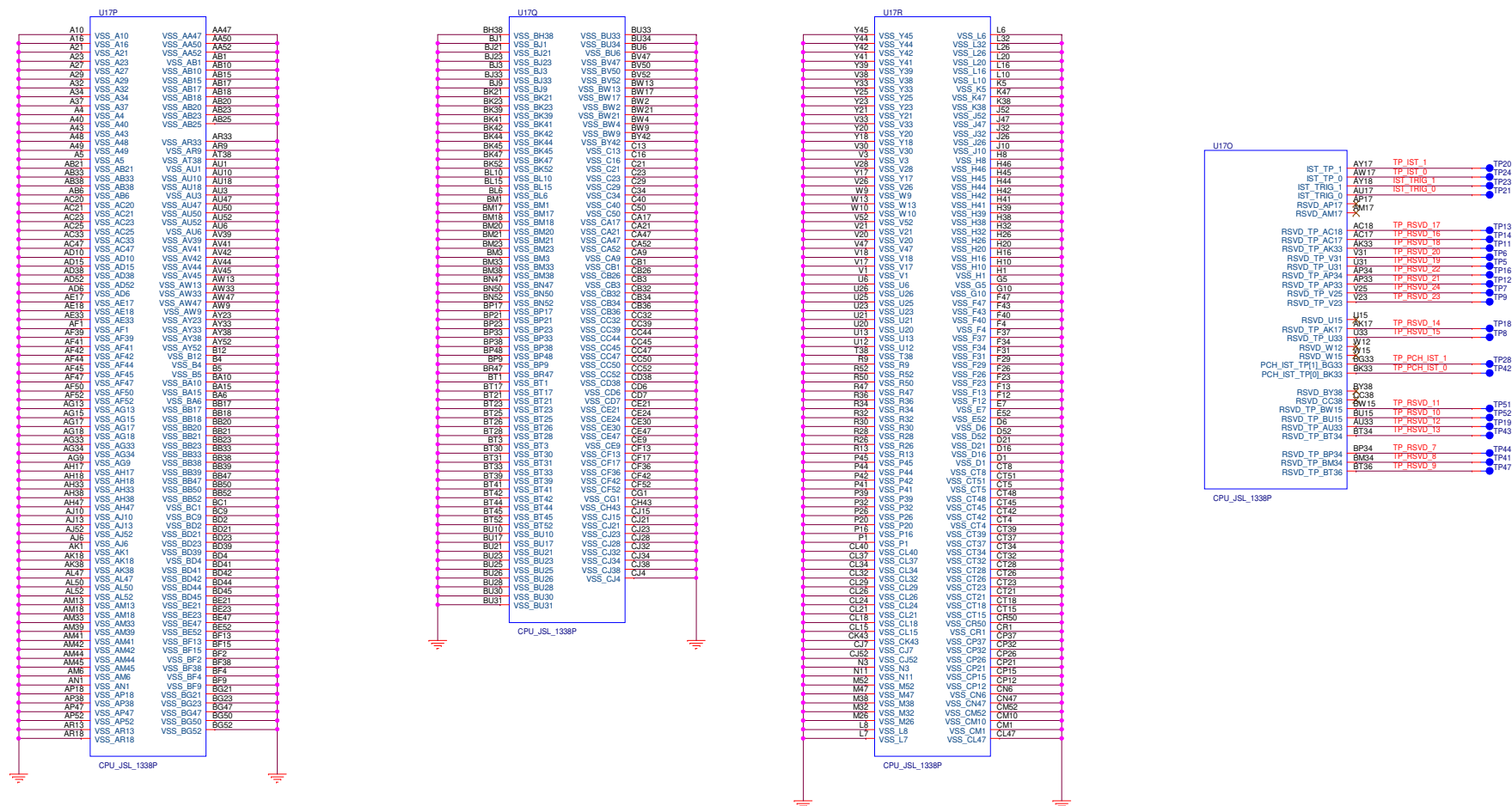
0717 Correct the description

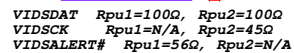
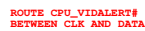




Rail	Voltage	Ic(max)	
VCCIN	0 V(MIN)-2 V(MAX)	35 A	VDC
VCCIN_Aux	1.65 or 1.8 V -Active 1.1 V -Retention Off - Idle States	24 A	VDC
VDDQ	1.2 V (DDR4)	3.5 A	VDC
VCCPRIM_3P3	3.3 V	0.232 A	VDC
VCCPRIM_1P8	1.8 V	0.089 A	VDC
VCC_VINEXT_IP05 (Optional)	1.05 V or 0.76 V	0.5 A	
VCC_VIPOSEXT_IP05 (Optional)	1.05 V	0.5 A	
VCCIO_EXT	1 V (Type)	5 A	VDC
VCCPLL	1.05 V	0.1 A	
VCCST	1.05 V	0.6 A	
VCC_OUT_RET_IP05	1.05 V	0.7 A	PCH FR
VCCSTG	1.05 V	0.15 A	PCH FR
VCCSTG_OUT	1.05 V	0.15 A	PCH FR
VCCLOSTD0_OP05	0.85 V		
VCCPRIM_1P05	1.05 V		PCH FR
VCCA_CLKD0_IP8	1.8 V	0.12 A	
VCCDPHY_1P24	1.24 V		
VCCOPPWR	1.8 V / 3.3 V	0.000337 A	
VCC1P8A	1.8 V	0.00337 A	
VCCRTC	3 V	0.001 A	
VCCPLL_OC	1.1 V / 1.2 V	0.1 A	
VCCSPI	1.8 V / 3.3 V	0.003 A	
VCCSDW_3P3	3.3 V	0.001 A	VDC

(CPU)





Volume Segment ICL U42

0617 Ruff 538/R372/R319 , Un-stuff D27 for Modern Standby
0731 Add & Reserve D38 for Power Optimized design on Modern-Standby
0623 Use SUSCE to control VCCST_EN for stuff R78000 only in the future instead of a bunch of parts
If VCCST is enabled by PMC_SLP_S4_N, no power gate is required for VCCPLL_OC and it can be merged with VDDQ directly. (P06,451)

0629 Connect U25.5 to +3V_S5 because of VIH (VID is +1.8V_S5)
0623_2 Change footprint of U15,U18 to "not353-2_1-65-5p"

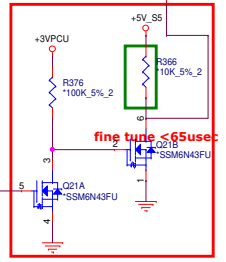
[2,3,5,7,9,20,21,24,25,28,29,30,31,33,34]
[5,17,18,20,22,25,26,27,28]
[16,26,28,31,32,33]
[7,9,11,27,32]
[8,9]
[2,9,13,14,31,34]
[9,34]
[6,9,22,25,33,34]
[9,34]

+3V_S5
+3VPCU
+5V_S5
+VCCST
+VCC1.05_OUT_FET
+1.2VSUS
+VCCPLL_OC
+1.8V_S5
+VCC1P8A

12

Volume Segment VCCST: 0.65A ≤ 65us full load ready

VCCST is that it needs to be on whenever VCCIN_AUX is on.

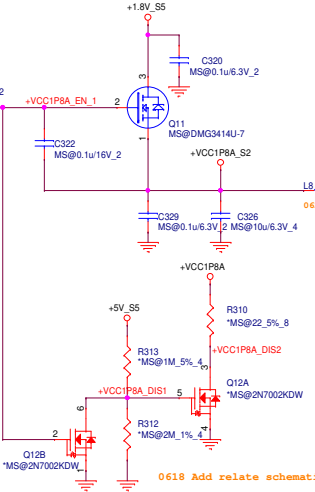
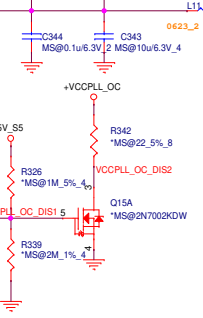
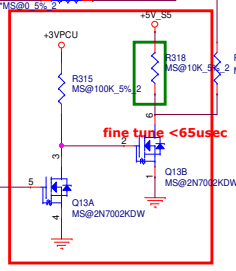


0907 Change Q21 from 2N7002KDW to SSM6N43FU by Vgs threshold
0921 DNB Q21,R376,R366 for un-using

0921 Add MS@ on VCCPLL_OC & VCC1P8A parts C10: turn off VCCPLL_OC , VCC1P8A

Max: 0.1A ≤ 65us, full load ready

Max:0.7A ≤ 65us full load ready

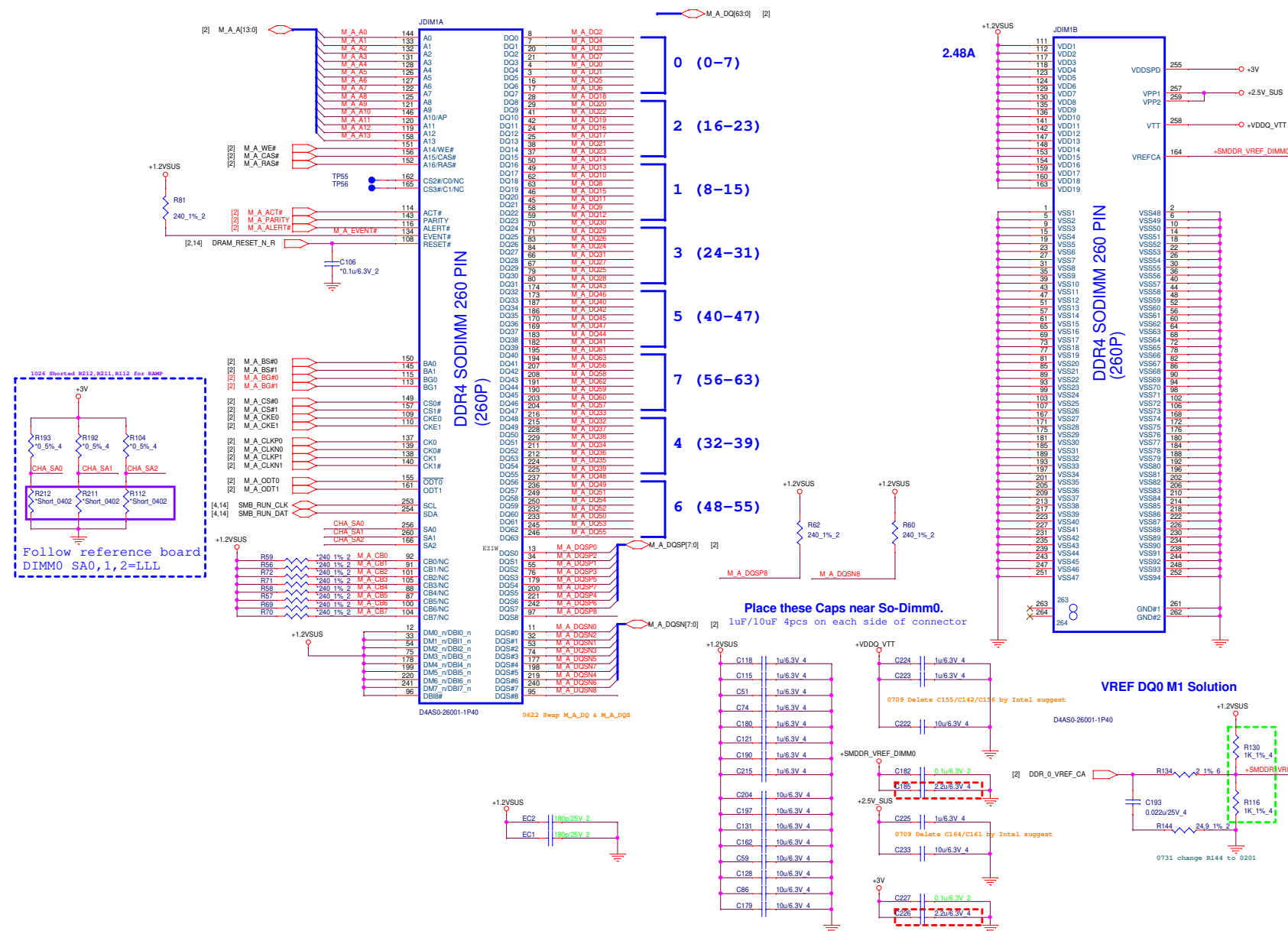


0618 Add relate schematic for power-on timing



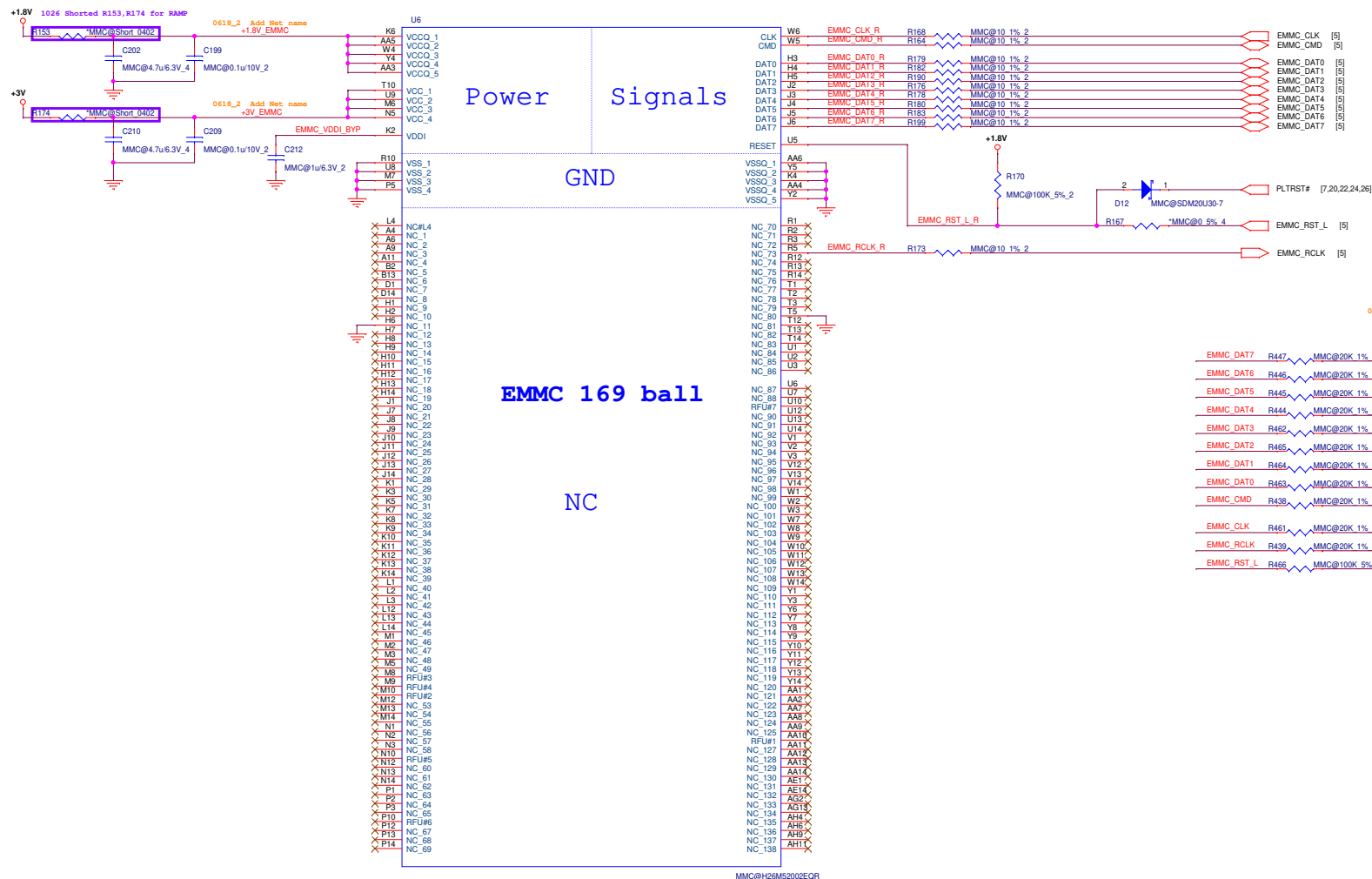
PROJECT : G7AL
Quanta Computer Inc.

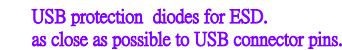
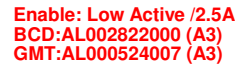
Size C	Document Number +1.0V/+VCCSTPLL	Rev 1A
Date: Thursday, November 19, 2020	Sheet 12 of 37	



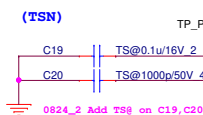
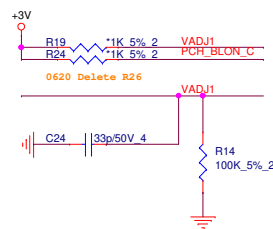
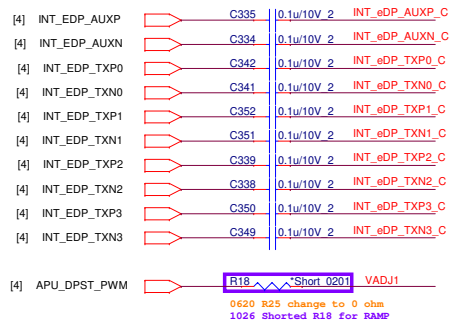
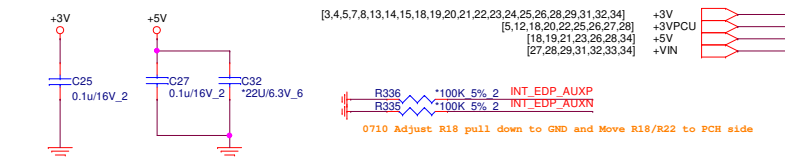
(MMC)

[18,22,25,34] +1.8V
[3,4,5,7,8,13,14,17,18,19,20,21,22,23,24,25,26,28,29,31,32,34] +3V



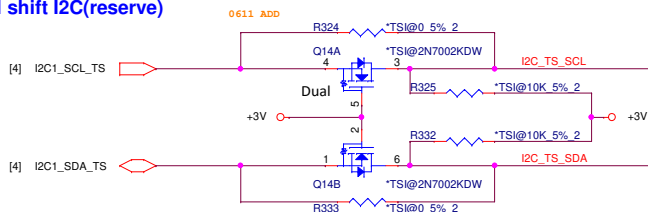


(LDS)



Touch screen level shift I2C(reserve)

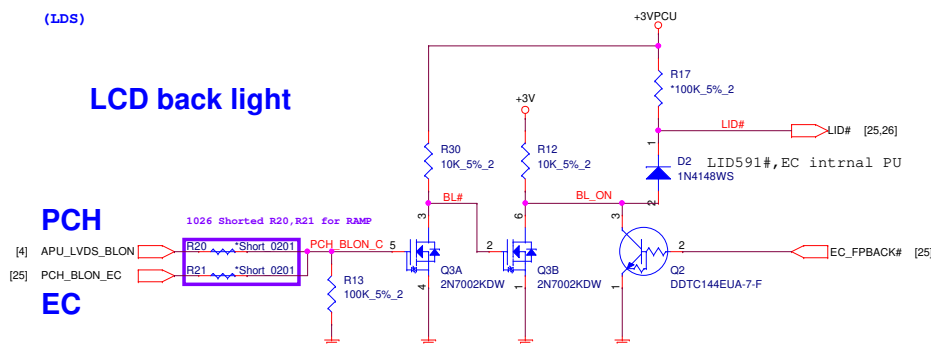
(TSN)



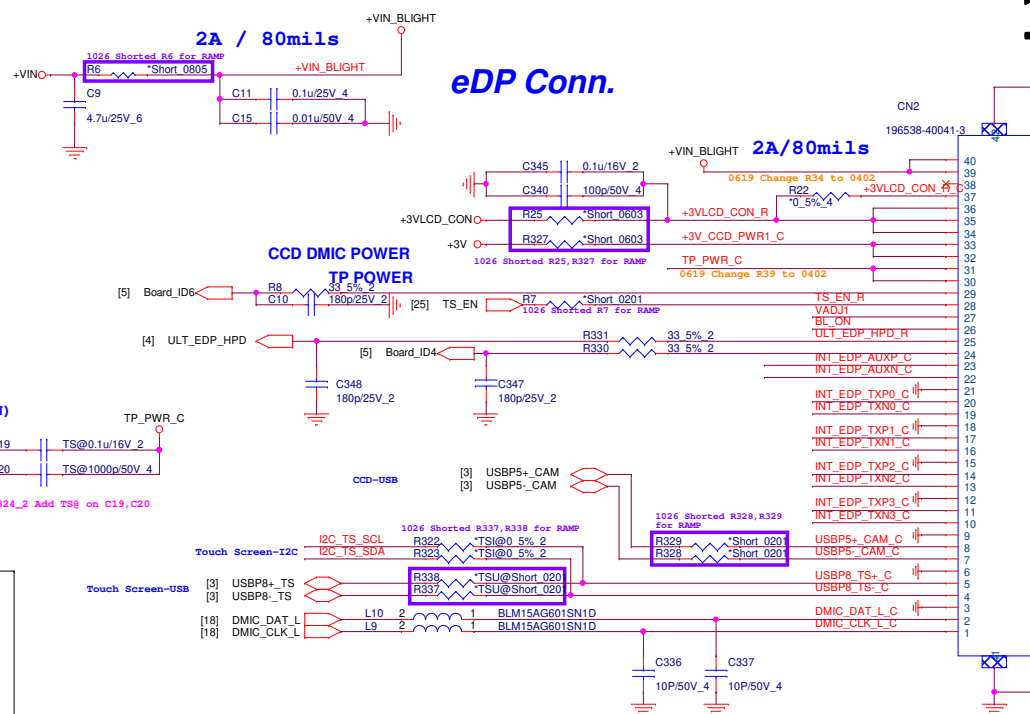
LCD back light

PCH

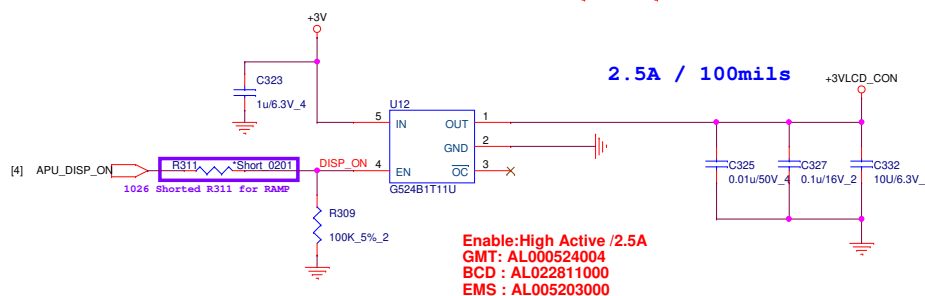
EC



eDP Conn.

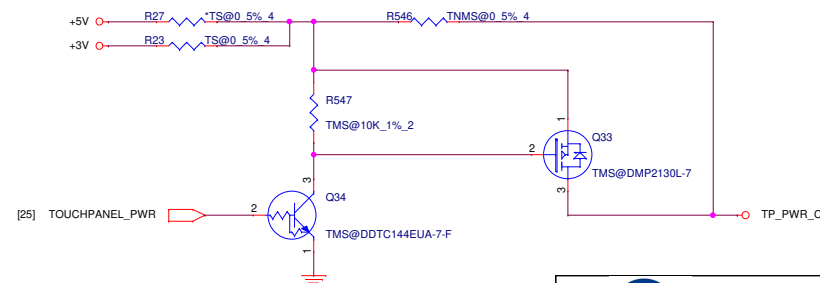


2.5A / 100mils

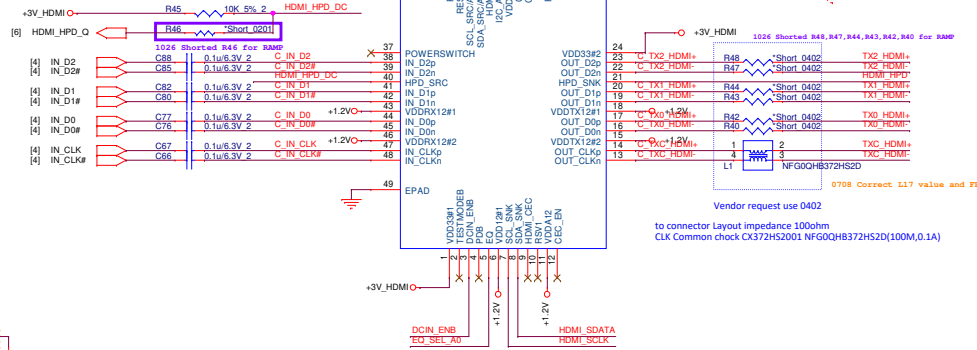


Touch Screen Power Control for Modern Standby (MS@)

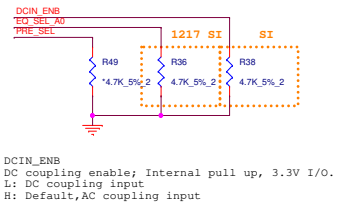
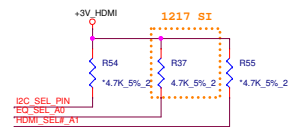
```
0807 Add Power control on Touch panel power to support Modern Standby
0810 Correct the value to "TMS@" & "TNMS@"
```



HDMI_HPD PD100K @ APU side



PS8409 strap pin

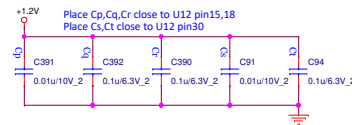
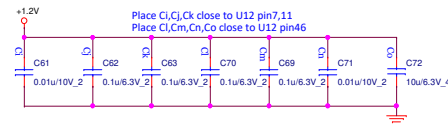


EQ_SEL_A0
Receiver equalization setting; Internal pull up, 3.3V I/O.
L: Compensation for channel loss up to 13dB
H: Default, Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

PRE_SEL
Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

HDMI_SEL_A1
HDMI_ID enable; Internal pull down, 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

I2C_SEL_PIN
I2C Slave Address selection; Internal pull down, 3.3V I/O.
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDf.



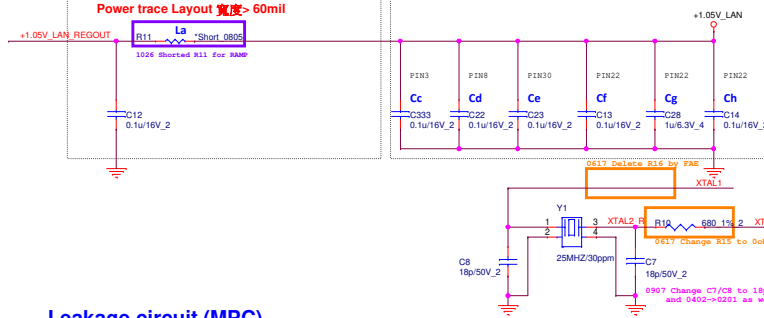
RTL8111H-CG (LAN)

20

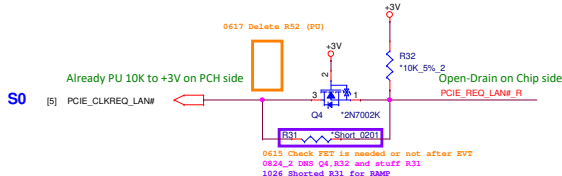
For LDO mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca, Cb

RTL8111HS
the switching regulator 1.0V output pin (REGOUT)
must be connected only to DVDD10 and AVDD10

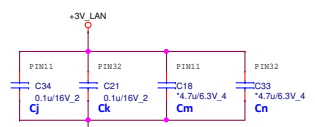
- * Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8, 30
- * Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)



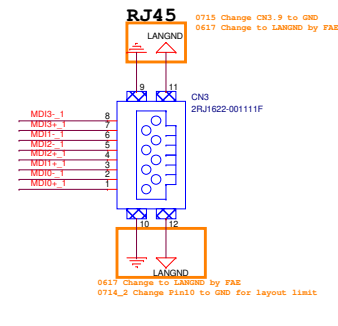
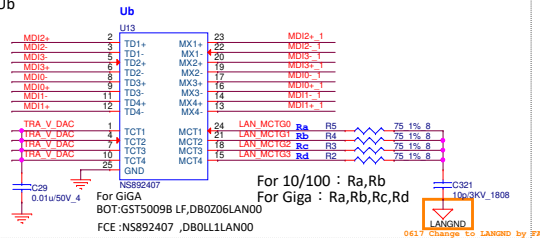
Leakage circuit (MPC)



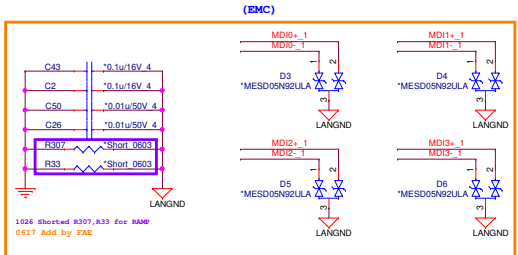
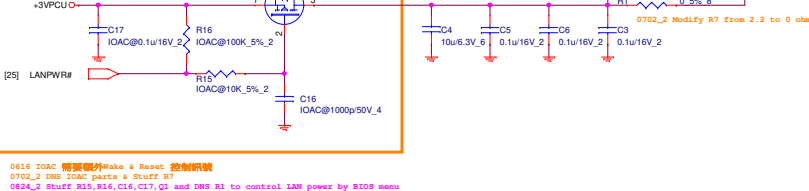
- * Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8107ESH-CG/RTL8111HSH-CG
- * For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



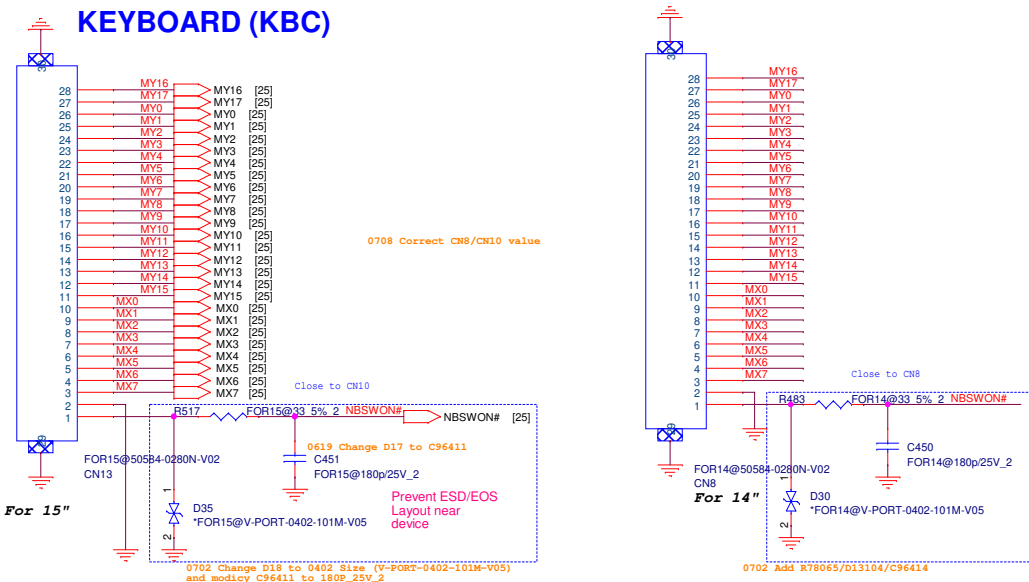
For Giga : Ub



LAN Wake Power Control (Control by BIOS Menu)



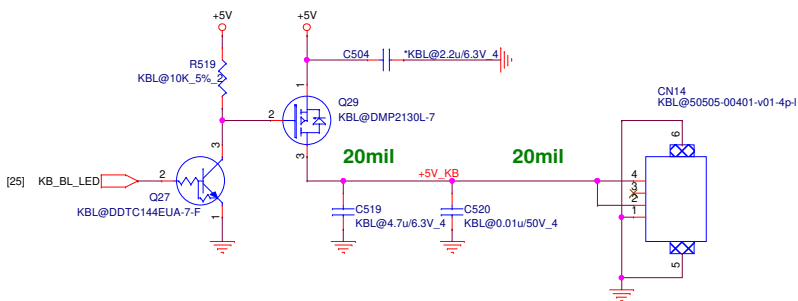
KEYBOARD (KBC)



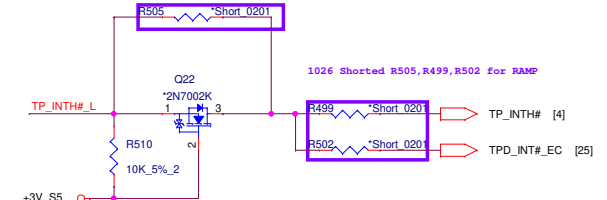
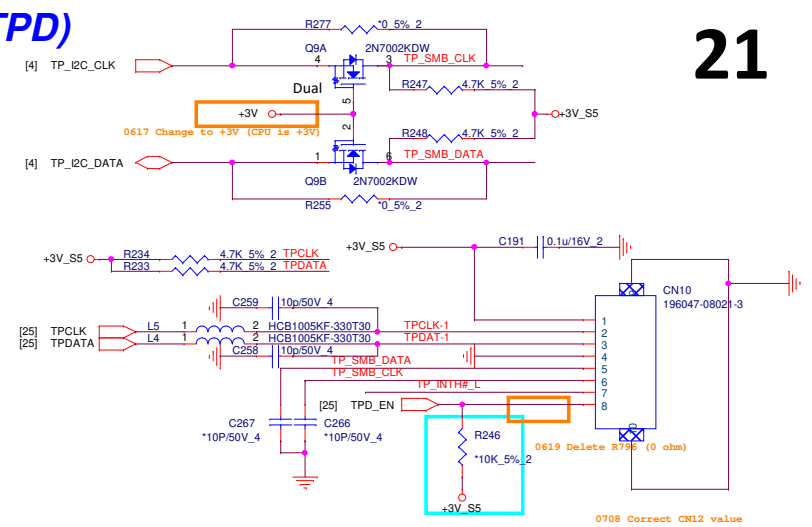
(EMC)

MY5	C285	220p/25V_2
MY6	C286	220p/25V_2
MY3	C283	220p/25V_2
MY7	C287	220p/25V_2
MY8	C288	220p/25V_2
MY9	C289	220p/25V_2
MY10	C290	220p/25V_2
MY11	C291	220p/25V_2
MY1	C281	220p/25V_2
MY2	C282	220p/25V_2
MY4	C284	220p/25V_2
MY0	C280	220p/25V_2
MX4	C494	220p/25V_2
MX6	C496	220p/25V_2
MX3	C493	220p/25V_2
MX2	C492	220p/25V_2
MX7	C497	220p/25V_2
MX0	C501	220p/25V_2
MX5	C495	220p/25V_2
MX1	C491	220p/25V_2
MY12	C292	220p/25V_2
MY13	C293	220p/25V_2
MY14	C294	220p/25V_2
MY15	C500	220p/25V_2
MY16	C278	220p/25V_2
MY17	C279	220p/25V_2

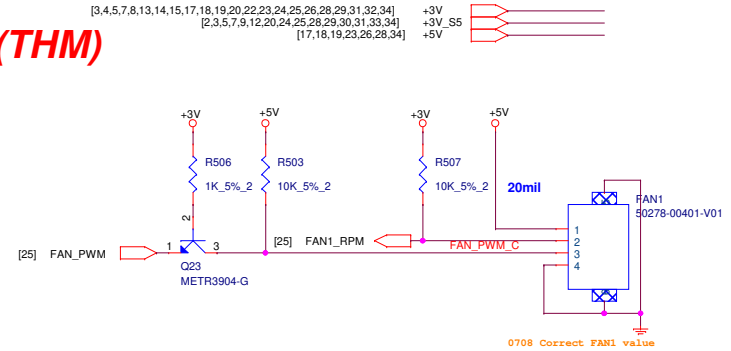
KB_BL LED (KBL)



Touch Pad (TPD)



FAN (THM)



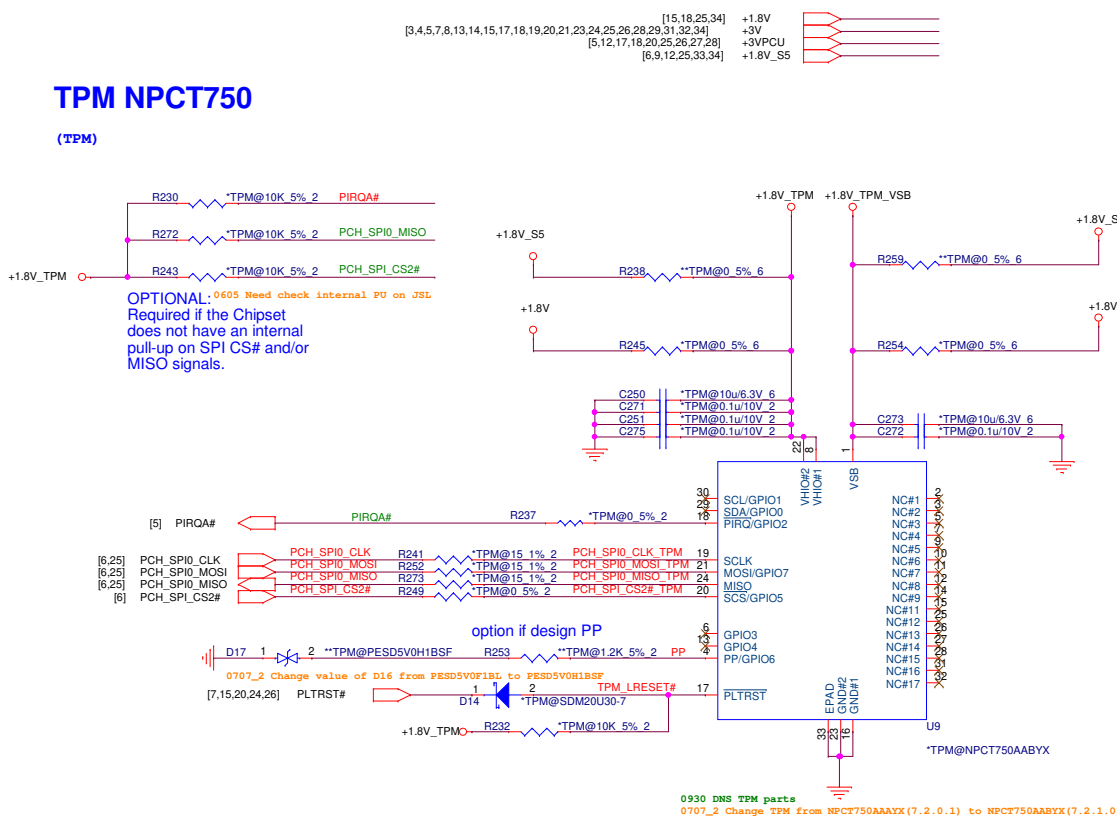
Quanta Computer Inc.
PROJECT : Z8Y

Size	Document Number	Rev
	KB/TP/FAN	1A

Date: Thursday, November 19, 2020 Sheet 21 of 37

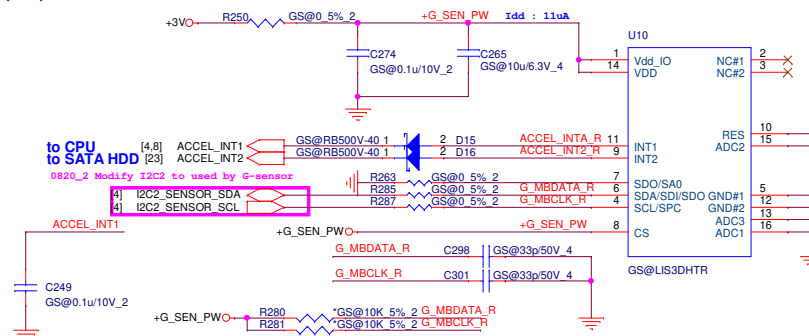
TPM NPCT750

(TPM)



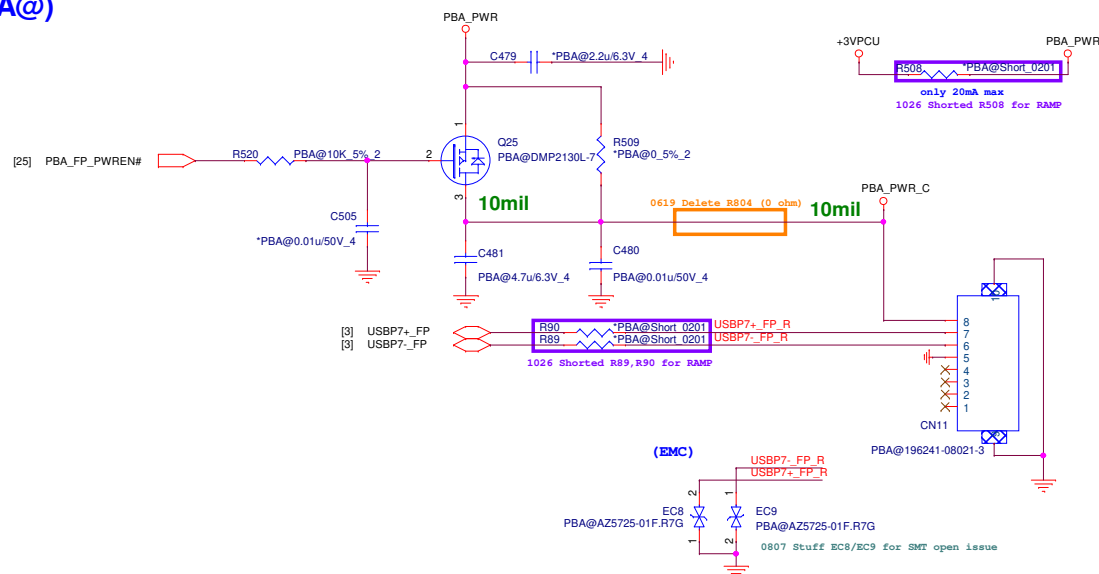
G-sensor

(ACS)



PBA (PBA@)

(FPD)



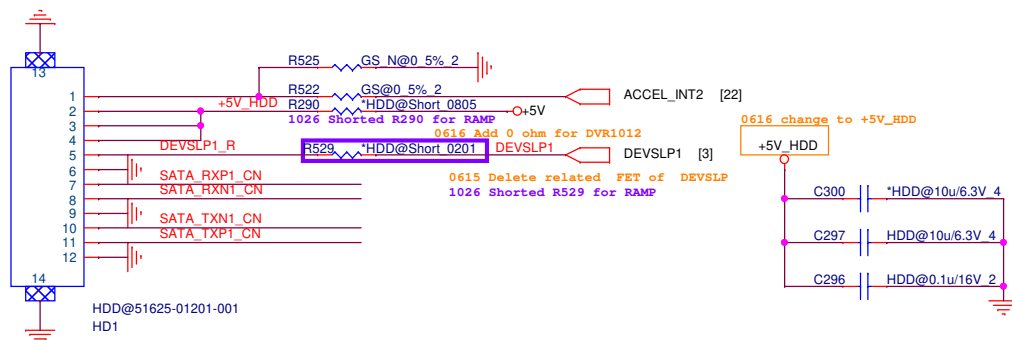
SATA HDD & LED

[17,18,19,21,26,28,34] +5V
[3,4,5,7,8,13,14,15,17,18,19,20,21,22,24,25,26,28,29,31,32,34] +3V



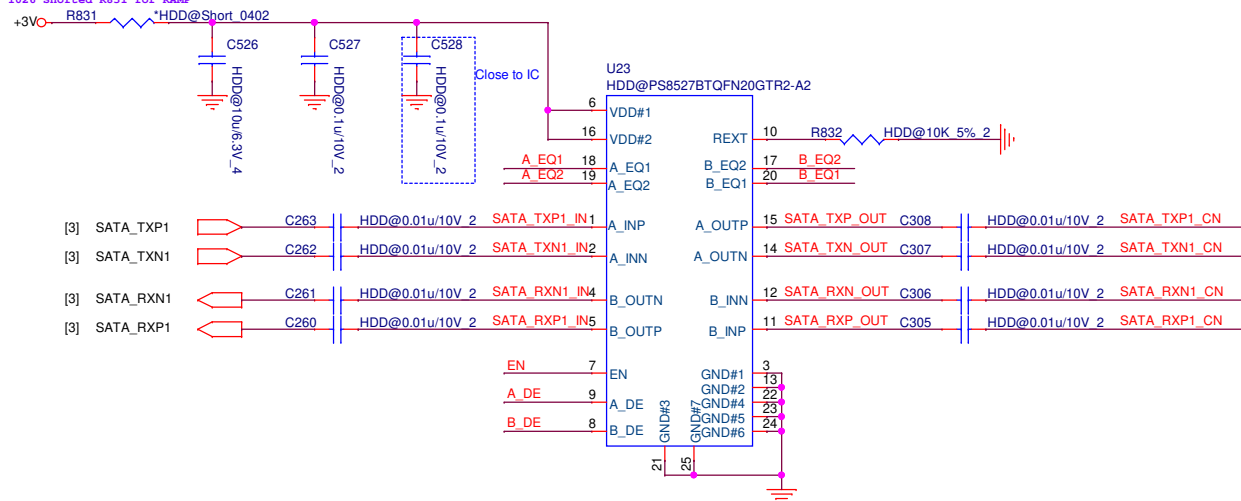
23

(HDD)



SATA HDD Re-driver

0827 Change Redriver to PDT---PS8527BTQFN20GTR2-A2
1026 Shorted R831 for RAMP

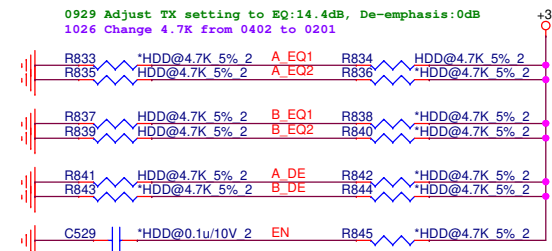


Equalization level setting for Channel x(x=A/B), internally tied to VDD/2 (default:12.2dB)
[x_EQ2, x_EQ1] ==

L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB (Setting for now)
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)
[x_DE] ==

M: -3.5dB
L: 0 dB (Setting for Now)
H: -6dB



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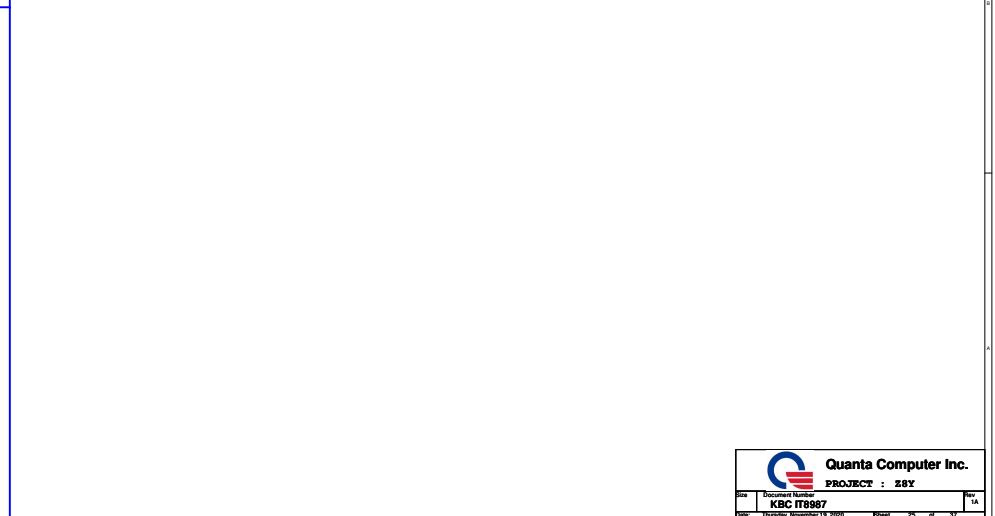
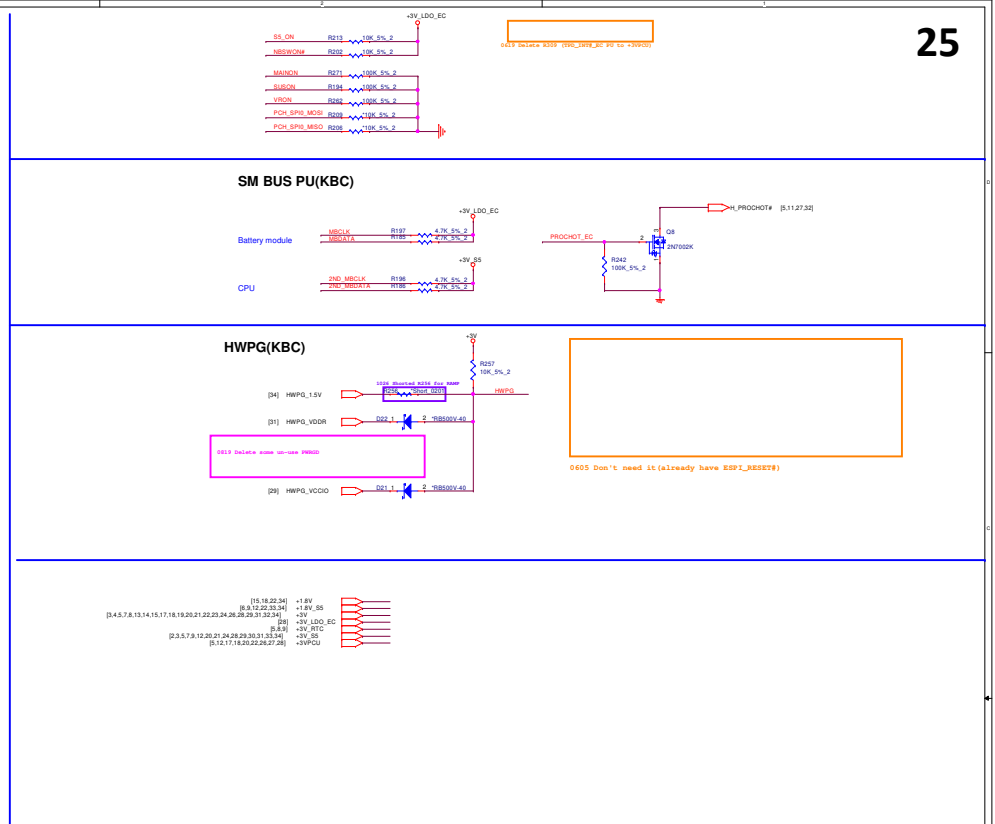
Size	Document Number	Rev
	HDD/ ODD	1A

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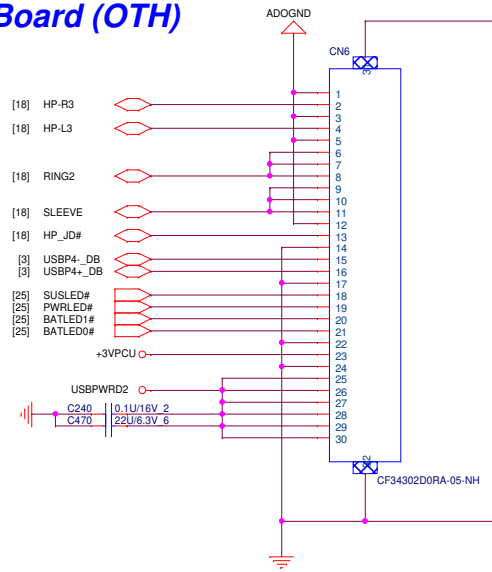


(NGF)

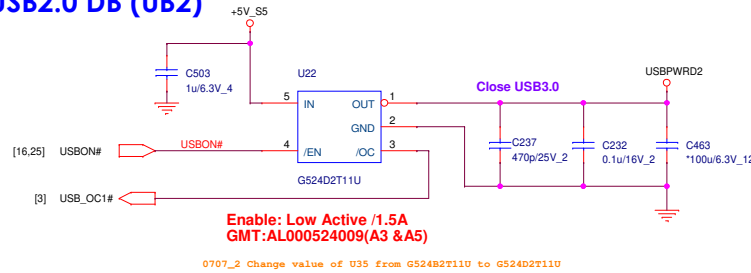




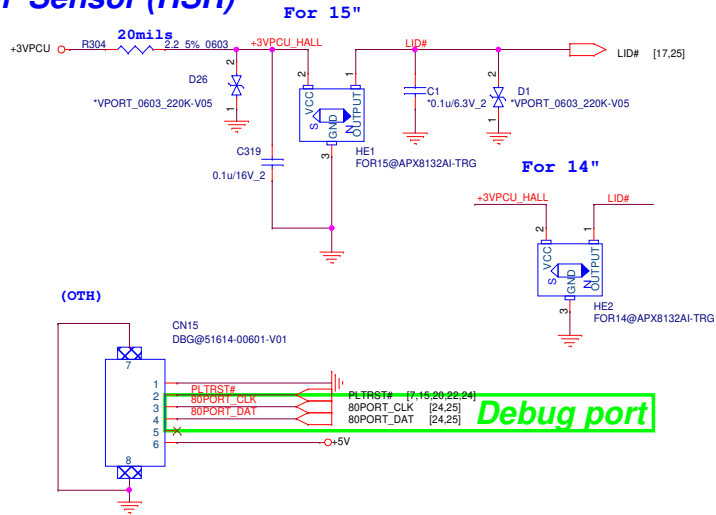
USB Board (OTH)



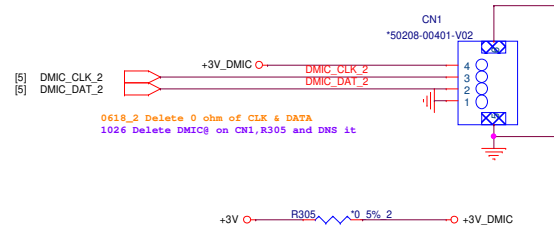
USB2.0 DB (UB2)



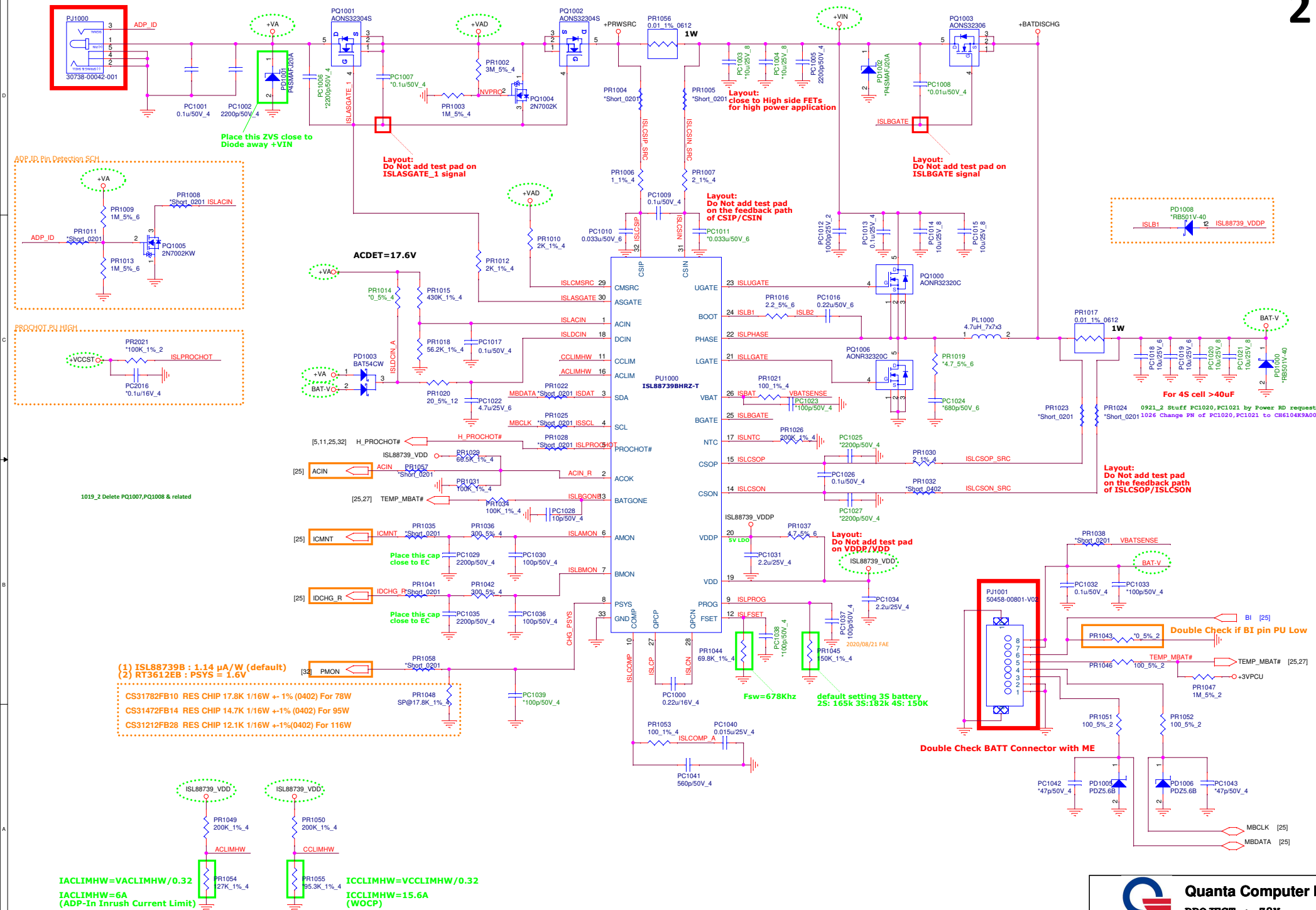
Hall Sensor (HSR)

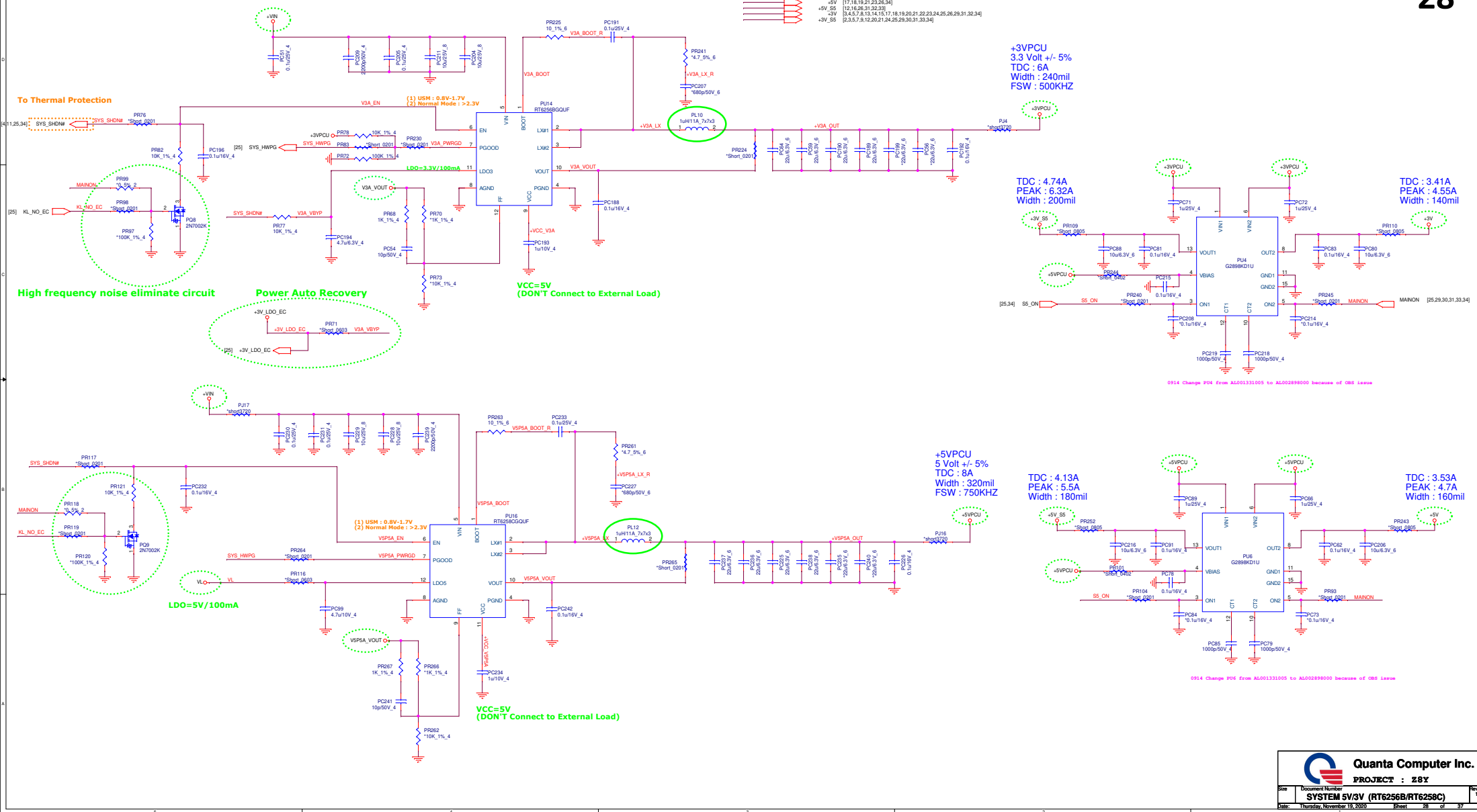


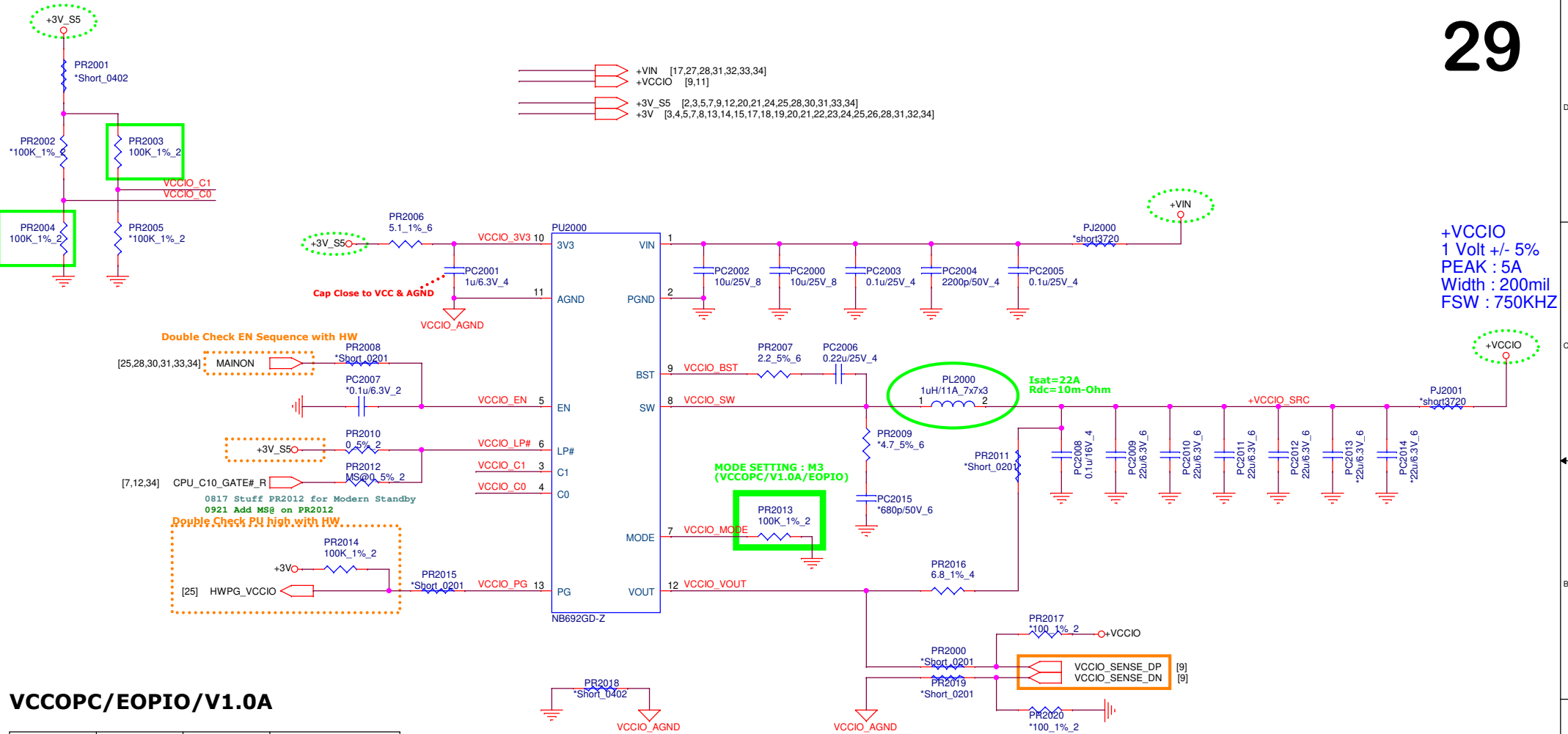
3rd DMIC (MIC)



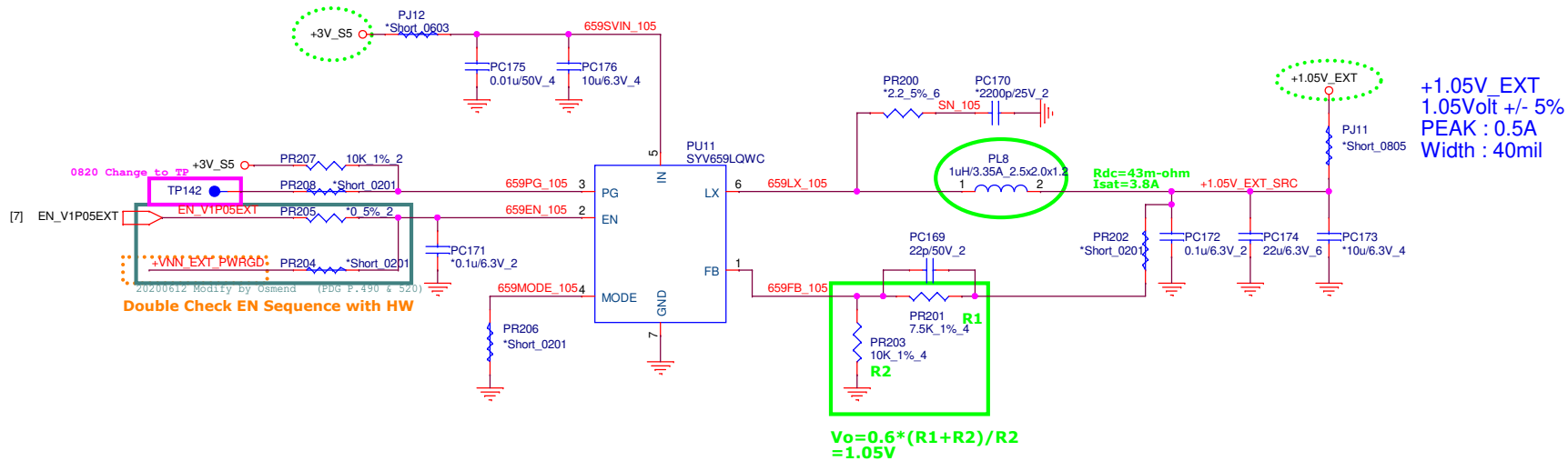
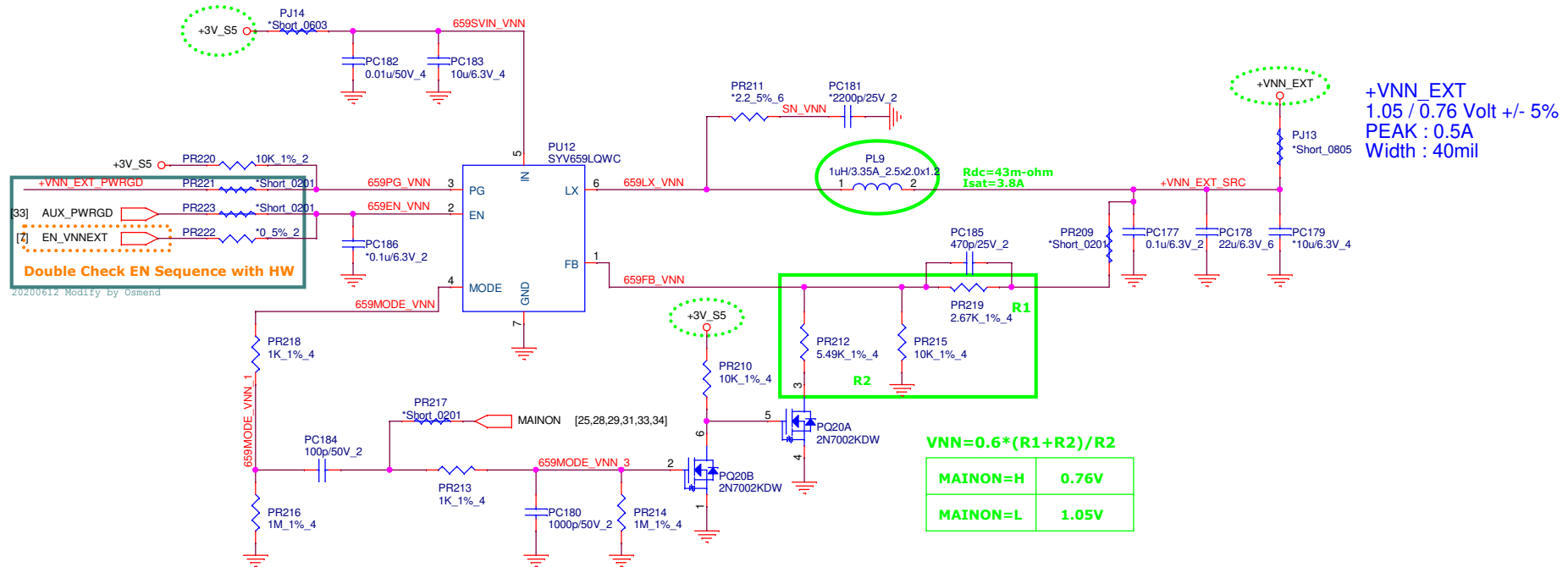
Double Check DC Jack with ME

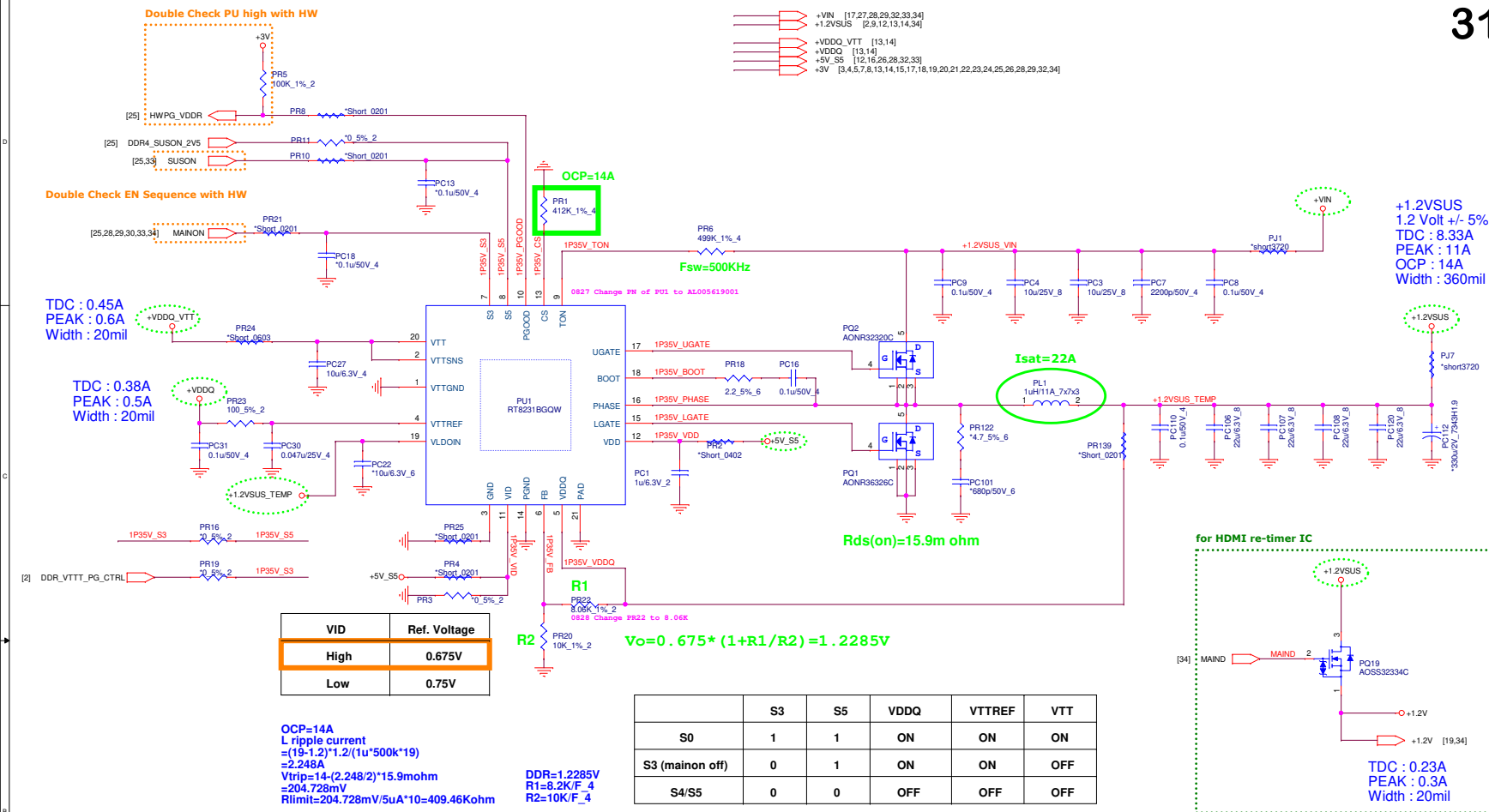




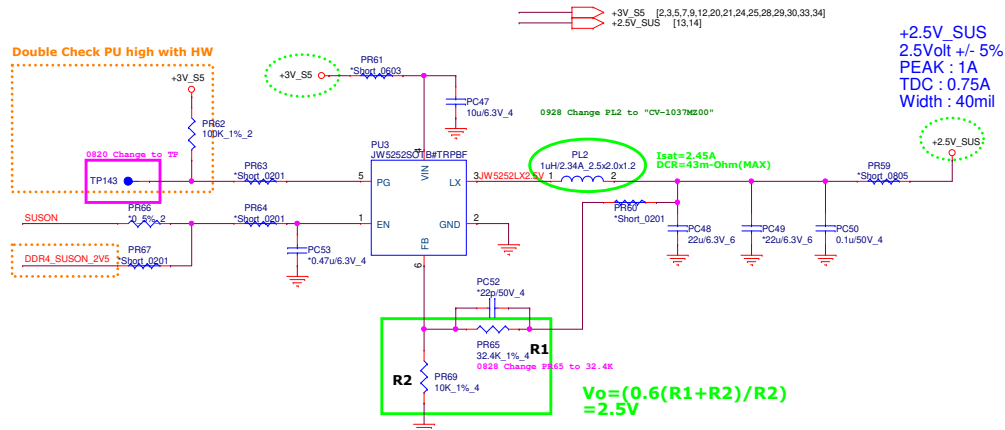


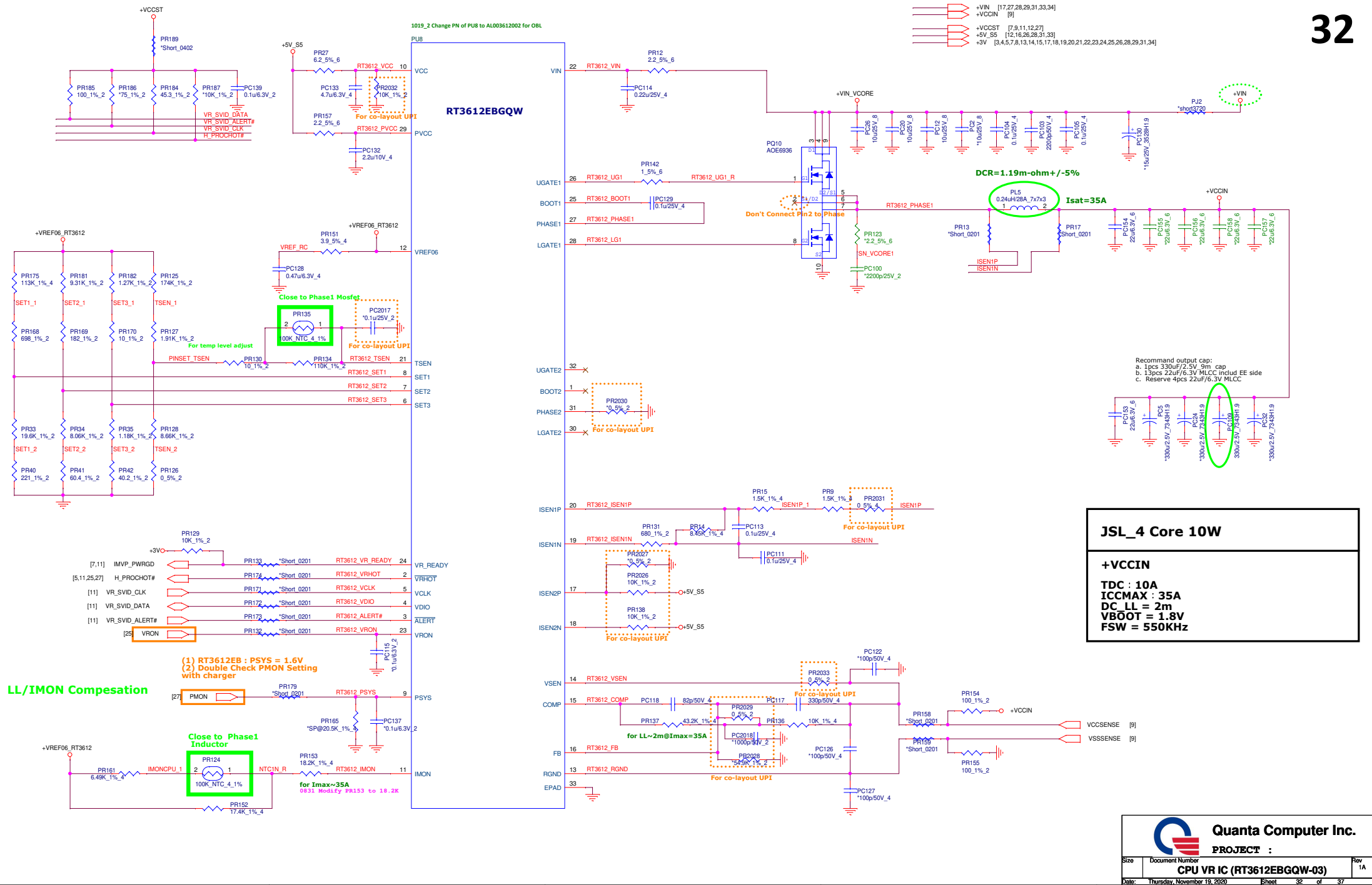
+3V_S5 [2,3,5,7,9,12,20,21,24,25,28,29,31,33,34]
 +VNN_EXT [9]
 +1.05V_EXT [9]

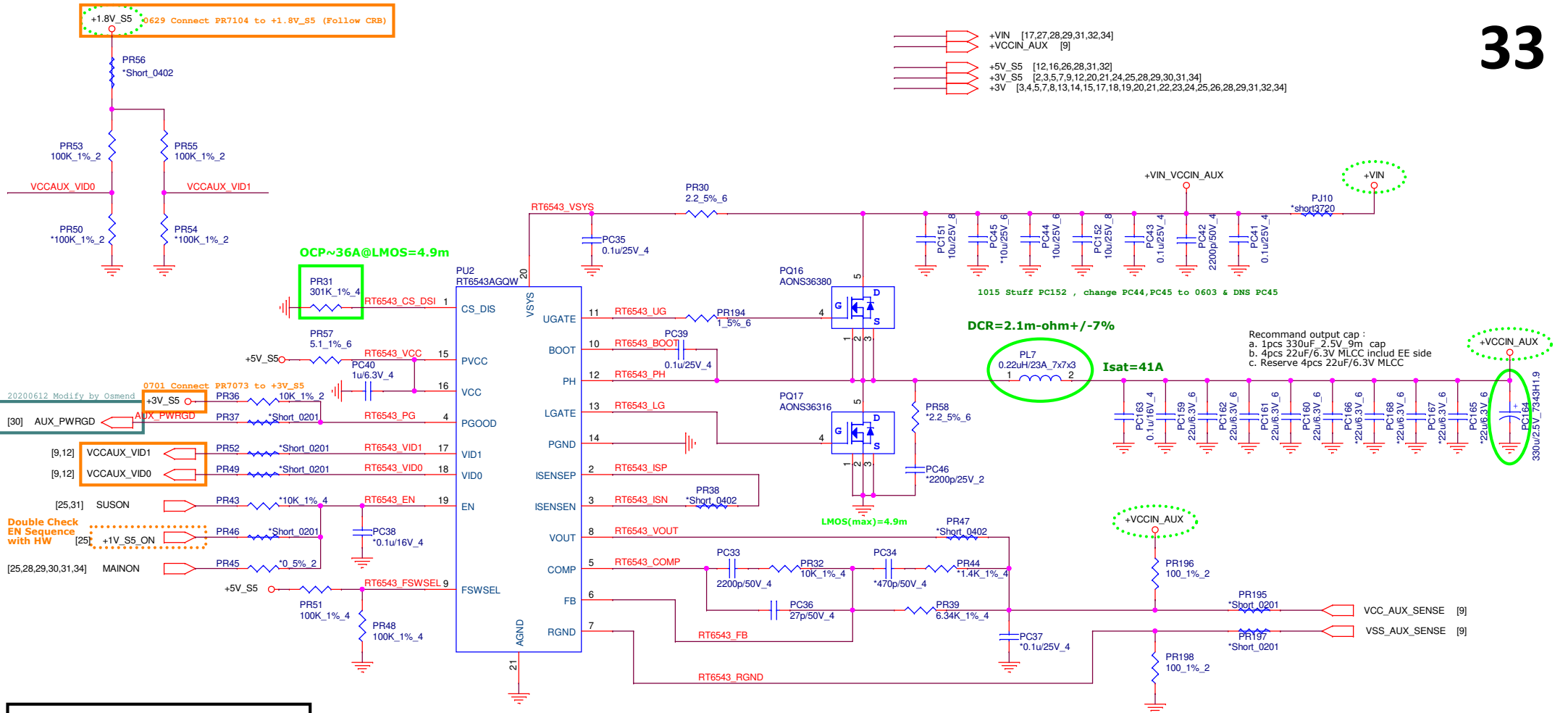




+2.5VSUS Power Rail For DDR4







+VCCIN_AUX
JSL_4 Core 10W

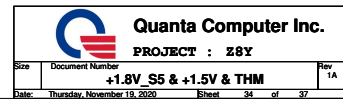
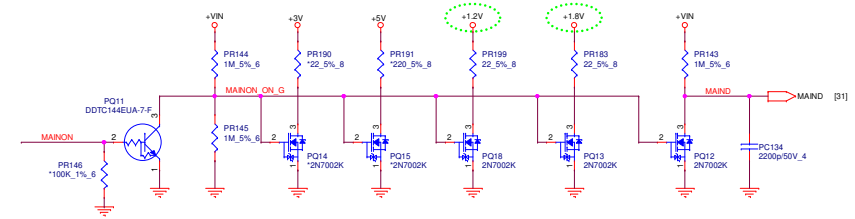
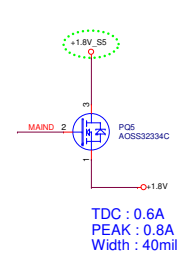
TDC : 4A
ICCMAX : 24A
LL = 0m
VBOOT = 1.8V



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PROJECT :

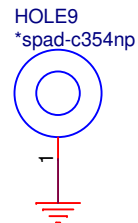
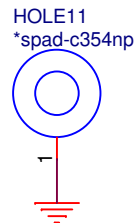
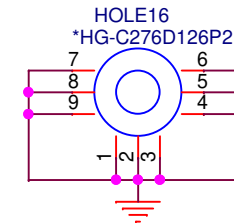
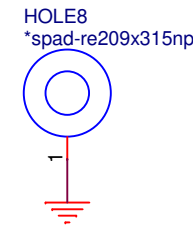
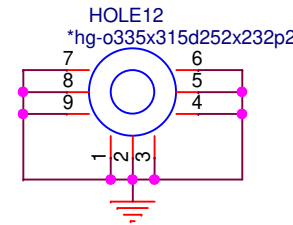
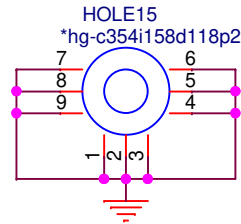
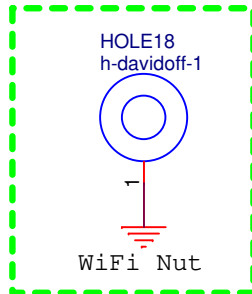
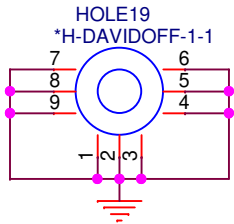
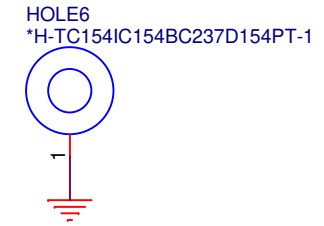
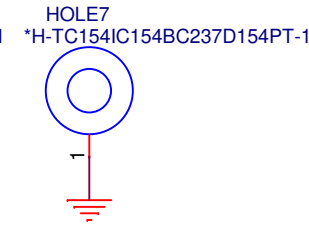
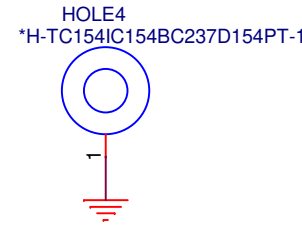
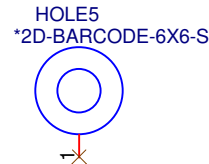
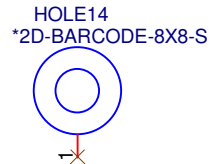
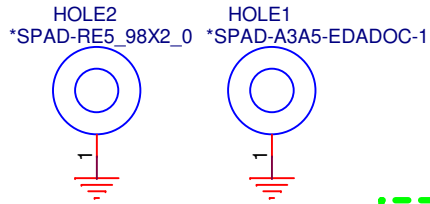
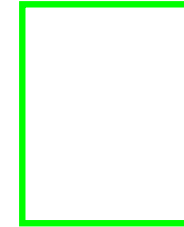
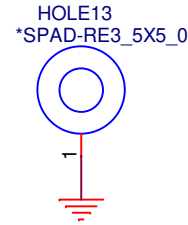
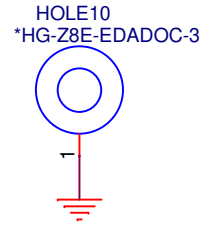
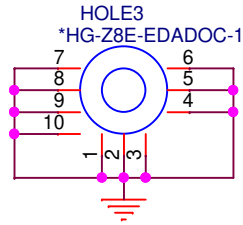
Size	Document Number	Rev
	VCCIN_AUX IC (RT6543AGQW)	1A
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Hole

35

remove HOLE12 as Z8E



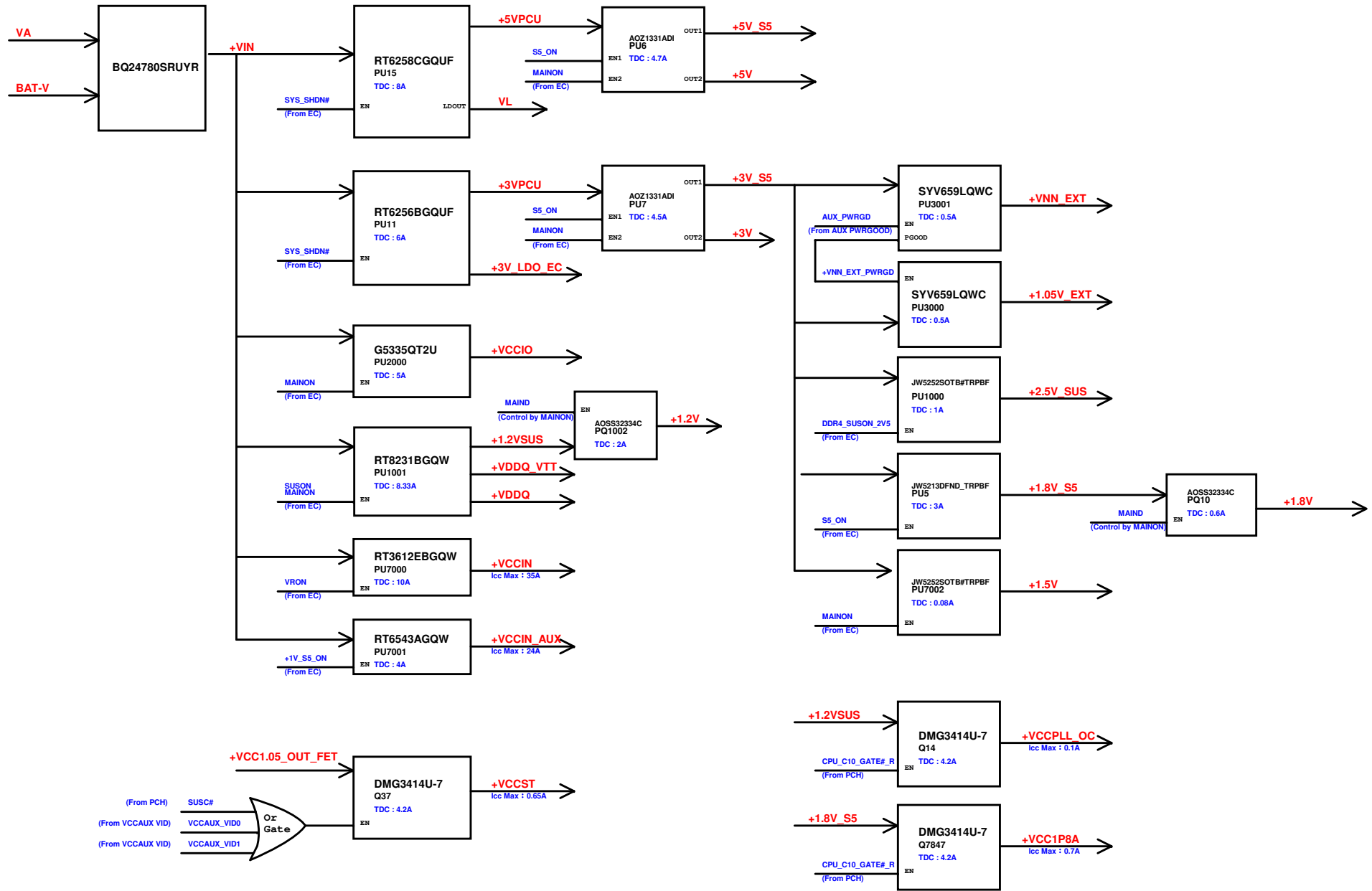
0618 Delete Hole3/Hole10/Hole15



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	Hole	1A
Date:	Thursday, November 19, 2020	Sheet 35 of 37



Stage	Date	CHANGE LIST
A	20191005	1. first released
C		
MP		